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Measurement and Reporting of Alpha Particles and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices

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MEASUREMENT AND REPORTING OF ALPHA PARTICLE AND TERRESTRIAL COSMIC RAY INDUCED SOFT ERRORS IN SEMICONDUCTOR DEVICES

Contents

Foreword

This specification defines the standard requirements and procedures for terrestrial soft-error-rate (SER) testing of integrated circuits and reporting of results. Both real-time (unaccelerated) and accelerated testing procedures are described. At terrestrial, Earth-based altitudes, the predominant sources of radiation include both cosmic-ray radiation and alpha-particle radiation from radioisotopic impurities in the package and chip materials. An overall assessment of a device's SER is complete, ***only*** when an unaccelerated test is done, ***or*** accelerated SER data for the alpha-particle component ***and*** the cosmic-radiation component has been obtained.

The procedures apply primarily to memory devices -- DRAMs and SRAMs -- but with some adjustments can be used for logic devices.

Annexes A, C, and D are informative; annexes B, E, and F are normative.

Introduction

Soft errors are nondestructive functional errors induced by particle strikes. This includes single-event upset (SEU), multiple-bit upset, and transients that may induce functional errors in nearby circuits. In general, soft errors may be induced by alpha particles emitted from radioactive impurities in materials nearby the sensitive volume, such as packaging, solder bumps, etc., and by radiation products from (cosmic-ray-induced) atmospheric neutrons.

There are two basic methods to determine a product's SER. One is to test a large number of actual production devices for a long enough period of time (weeks or months) until enough soft errors have been accumulated to give a reasonably confident estimate of the SER. This is generally referred to as a real-time system SER (SSER) test. SSER testing has the advantage of being a direct measurement of the actual product SER requiring no extrapolation, assumptions, or special experimental structures, equipment, etc. However, SSER testing requires systems capable of monitoring hundreds or thousands of devices in parallel, for long periods of time. Additionally, a single SSER test does not identify the specific cause of the observed soft errors.

The other method commonly employed to allow more rapid SER estimations and to clarify the source of errors is accelerated-SER (ASER) testing. In ASER testing, devices are exposed to a specific radiation source whose intensity and energy spectrum is defined and typically much higher than the ambient levels of radiation the device would normally encounter. As the name implies, ASER allows useful data to be obtained in a fraction of the time required by real-time, unaccelerated SSER testing. Only a few units are needed and complete evaluations can often be done in a few hours or days instead of weeks or months. The disadvantages of ASER are that the results must be extrapolated to use conditions and that several different radiation sources ***must*** be used to ensure that the estimation accounts for soft errors induced by both alpha particle and cosmic-ray-neutron events.

MEASUREMENT AND REPORTING OF ALPHA PARTICLE AND TERRESTRIAL COSMIC RAY INDUCED SOFT ERRORS IN SEMICONDUCTOR DEVICES

(From JEDEC Board Ballot JCB-01-39, formulated under the cognizance of the JC-13.4 Subcommittee on Radiation Hardness: Assurance and Characterization.)

1 Scope

This standard specification covers soft errors due to alpha particles and atmospheric neutrons. Clause 3 covers real-time or unaccelerated SSER measurements, Clause 4 covers alpha particle ASER measurements, and Clause 5 covers terrestrial cosmic ray ASER test procedures.

This specification defines the standard requirements and procedures for terrestrial SER testing (including SSER and ASER) of integrated circuits and a standardized methodology for reporting the results of the tests.

The procedures apply primarily to memory devices -- DRAMs and SRAMs -- but with some adjustments can be used for logic devices.

Warning These tests may involve hazardous materials, operations, and equipment. Test hardware and parts may become radioactive when exposed to ion and neutron radiation, or when recoil fragments or larger fragments of the radioisotope escape the alpha source encapsulation. It is the responsibility of the user of this test method in consultation with radiation safety personnel to establish the appropriate safety and health practices and to determine the applicability of regulatory limitations prior to use.

2 Terms and definitions

2.1 ASER: Accelerated soft error rate, i.e., one obtained in the presence of ionizing radiation source.

2.2 ATE: Automatic test equipment

2.3 Critical charge (Q_c): The minimum charge collected at a sensitive node due to a particle strike that produces a soft error. In the DRAM cell the critical charge decreases with time until the cell is refreshed since leakage mechanisms are draining the storage capacitor of its charge. In the case of SRAM or latches, the critical charge increases with time since in most cases the nodes are driven (albiet weakly). If a device node collects charge in excess of its critical charge after an ionizing radiation event, the data state of that circuit will be upset.

2.4 DUT: Device Under Test.

2.5 ECC: Error Correction Code, sometimes called Error Detection and Correction (EDAC).

2.6 FIT: Failure In Time; one FIT is one failure in 10^9 device-hours.

2 Terms and definitions (cont'd)

2.7 Fluence The particle flux integrated over the time required for the entire run, expressed as particles/cm^2.

2.8 Flux: The number of particles passing through a one square centimeter area per unit time (particles/cm^2 s).

2.9 Sensitive volume: A region, or multiple regions, of a device from which deposited charge can be collected by device nodes, in such a manner as to produce SEU/SER.

2.10 Single-event upset (SEU): An event that induces a data error or upset in which the state of a latch or memory cell is reversed (one to zero, or vice versa).

2.11 Soft error: An SEU in a latch or memory cell that can be correctly rewritten. The error is "soft" because the circuit itself is not permanently damaged and behaves normally after the data state has been restored.

2.12 Soft error rate (SER): The rate that soft errors are occurring.

2.13 SSER: System soft error rate or unaccelerated SER; no radiation source present other than what is there naturally.

2.14 Hard error: A permanent circuit or device failure. The error is "hard" because the data is lost AND the circuit/device no longer functions properly, even after power reset and re-initialization. Hard errors are usually not an issue for alpha-particle events but can be caused by cosmic events such as gate rupture or destructive latch-up events.

2.15 Test vehicle: A circuit designed with the purpose of evaluating the soft error sensitivity of a particular process. This is not typically a product but is used to extrapolate to product SER.

2.16 Device: A packaged or integrated circuit (this could be either a test vehicle or an actual product)

2.17 Process: The manufacturing steps and methodologies used to fabricate an integrated circuit.

2.18 Product: A complete integrated circuit sold to satisfy a particular customer.

3 Real-time (unaccelerated) SSER test procedures

3.1 Background

3.1.1 Introduction

The most direct way to measure SER in a device is simply to observe it during its normal operation under standard operating conditions with no external sources of radiation except the normal ambient background radiation. The inherent problem with this approach is that the effective failure rate is so low that a single device would take decades to generate a statistically significant number of soft errors. To circumvent this limitation, real-time, unaccelerated SSER testing utilizes a very large number of devices in parallel to reduce the required test time. Chi-squared statistics (described in Annex A) are then applied to provide a confidence interval and to determine the test duration.

3.1.2 Guideline

The test method described below defines the requirements and procedures for SER testing without an ionizing source, i.e., only the natural ambient background radiation. Accelerated or ASER testing with alpha particles and neutron/proton radiation is dealt with in clauses 4 and 5, respectively.

3.1.3 Limits of test method

This test method is designed for the testing of SRAM and DRAM memory arrays, but could be adapted for use with other products. The SSER test algorithm and/or hardware must have allowances for separating actual soft errors from errors induced by system noise. Typically, the SSER test method does not discriminate between alpha particle and neutron induced soft errors.

In certain cases, such as running an SSER test in a cavern where the cosmic radiation contribution is minimized or, conversely, moving the system to a high altitude where the cosmic radiation contribution is increased, the SSER test can be used to infer contribution from alpha particles and from atmospheric neutrons.

In other cases, tests can be somewhat accelerated by use of reduced voltage. It is important to note, however, that SER voltage scaling is dependent on technology, device circuit design, and processing. There may be variation even from lot to lot for the same process. It is critical to define the specific SER to voltage (SER vs. power supply voltage) by accelerated SER tests performed prior to packaged, unaccelerated SSER testing at reduced voltage.

3.1.4 Goal of test method

The primary goal of SSER testing is to obtain a well-defined estimate of the total soft failure rate for products/devices using a uniform methodology.

3 Real-time (unaccelerated) SSER test procedures (cont'd)

3.1 Background (cont'd)

3.1.5 Warnings

This test does not involve any radioactive material, but a radiation survey should be taken of the test area to verify that the background radiation level is typical for the location as previous SER experiments may have contaminated the area. If possible, an accurate reading of the atmospheric neutron level should be made so that a reasonable benchmark can be established for the product.

3.2 Test facilities and equipment

3.2.1 Basic test requirement

The basic SSER test requirement is to monitor each DUT's output vector and continually verify that the output matches the expected output vector. A vector could simply be data stored within a memory array of a DUT, or the output vector could be a stream of data generated as an operation or sequence of operations performed by the DUT on an input vector (this would be relevant for processors, etc., that are not specifically related to this test standard). If the vector from the DUT does not match the expected vector, then a soft error may have occurred. The system consists of the input stimulus generator and response recorder that is designed to accommodate the specified device. Testing requires some sequence of writing data to the DUT, reading the data back, comparing the output data to the written data, and tabulating the number of detected errors.

3.2.2 DUT board hardware

SSER testing requires a DUT board capable of supporting a large number of DUTs. Several DUT boards maybe used in a single system. The boards are controlled by a computer driven system that monitors and communicates with the DUTs during the test interval.

3.2.3 Test hardware

The test cables should be short enough and designed with the proper shielding to allow sufficient test speeds without electrical noise problems in a noisy environment. The tester must be configured to do both static and dynamic testing. The following features are also desirable:

- the ability to adjust and monitor the temperature of the DUTs or at least the volume in which the DUT boards are located;

- the ability to monitor power supply current of individual DUTs to check for latchup (preferably the ability to individually remove power from latched-up DUTs should also be provided);

- operation at, or near, the rated clock cycle for the DUT.

3 Real-time (unaccelerated) SSER test procedures (cont'd)

3.2 Test facilities and equipment (cont'd)

3.2.4 Test software

The basic requirements for the DUT test system are as follows:

1) create test conditions for input into the DUT;

2) identify, record, and correct any errors based on the selected test conditions;

3) provide adequate fault coverage;

4) control device initialization and rudimentary functional checks;

5) select operation mode (dynamic or static operation) and provide resetting capability);

6) provide error detection and logging.

In addition to the previous requirements, the following features are also desirable:

1) bit error mapping and data processing, storage, and retrieval for display;

2) applicability to many device types, e.g., software control with programs written in a high-level language;

3) speed of operation and high duty factor. Generally, a computer-assisted tester design is implied by this characteristic;

4) real-time DUT data display capability providing a higher test throughput and allowing for more precise control of testing;

5) data reduction while tests are in progress (this feature is desirable for modification / optimization of test procedures in the light of data being acquired).

The basic test program for memories includes writing a pattern to the device and reading the device periodically during the test. The program should include several different patterns to investigate sensitivity. In general, the test program for memories or arrays of latches should include a pattern of ones, zeros, and internal checkerboard, as a minimum, since devices often have a preferred data state that is more robust.

3.3 Testing procedures

3.3.1 Pretest preparations

3.3.1.1 Standard operating procedure

Before beginning SSER testing it is important to ensure that all personnel are properly trained, that the test equipment has been properly setup, and that the test system is operating as expected. Setup conditions vary with each facility.

3.3.1.2 Test plan

A test plan shall be developed to support each test. The test plan will serve as a guide for the procedures and real time decisions to be made during the actual testing period. Since SSER testing typically involves a large number of devices and relatively long test times (weeks or months), a good test plan is crucial. It is extremely helpful to have some accelerated SER data (alpha particle and neutron) to get an estimate of the average failure rate. This average failure rate can then be used with chi-squared statistics to optimize the sample size and test duration so that the SSER results will be valid to the desired confidence interval.

3.3.1.3 Sample selection

Device-to-device variability for SSER is generally small for devices produced with the same masks and fabrication steps. However, the system user must be sure that the devices tested are equivalent to actual baseline production devices, because manufacturers often make process/design changes affecting SSER without changing the device's numerical designation. In general a minimum requirement to establish a product’s SSER is to run the test with roughly equal numbers of nominal devices from at least three different baseline lots. If a product is tested that has on-board error-correction codes/circuits (ECC) tests need to be run under two conditions, both with ECC enabled and with ECC disabled. If this is not possible, the fact that ECC is present must be included in the data sheet.

3.3.1.4 DUT preparation

The DUT package must be the final production package.

3.3.1.5 Effective neutron flux at the test location

When performing SSER testing, it is desirable that the neutron flux be estimated or measured. An estimate could be as simple as finding a reference of neutron fluxes over the world and comparing to the NYC flux levels used as a standard in this document (see Annex D). Another way would be to actually measure the neutron flux in the test location; however this is rather involved since several detection schemes are required to obtain counts over a large neutron energy range and there are many interferences and issues.

3.3 Testing procedures (cont'd)

3.3.2 Setup procedure

3.3.2.1 DUT handling

Special care must be taken in handling the DUTs used for SSER tests. All parts must be handled with the precautions for parts susceptible to damage from electrostatic discharge. The use of ground planes and straps is highly recommended whenever possible. If not in a production (encapsulated or hermetically sealed) package, a standard metal lid for the package should be attached with tape to ensure that the die is protected during handling and storage.

3.3.2.2 Test equipment location

The test equipment should be set up as close to the DUT holder as possible to avoid noise issues related to long cabling. Also ensure that cables are not physically blocking any areas accessed during the replacement of DUTs.

3.3.2.3 Tester check-out

A tester checkout should be performed with the equipment that will be used to perform the test, including all cables connected as they will be during the irradiation. After any major changes such as replacing the DUT, or changing the cabling arrangement, a short dry-run test should be run to verify proper operation of the devices and the test system. It is important to test the entire system, with all the DUTs in place for the some time in order to ensure tester integrity.

3.3.3 DUT testing

3.3.3.1 Load DUT

Place the desired population of DUTs in their sockets on each DUT board and run the test program to verify proper operation of all the DUTs. Adjust system and DUTs until the test program executes flawlessly on all DUTs in the test system.

3.3.3.3 General testing specifications

Keep the DUTs on test until the desired number of errors has been observed or until the appropriate test duration (determined by chi-square statistics and the required confidence intervals). A minimal test will include the following operations:

- Load DUTs.
- Verify correct test program execution and that all DUTs are nominal.
- Monitor error location and time of occurrence.

3.3 Testing procedures (cont'd)

3.3.3 DUT testing (cont'd)

3.3.3.4 DRAM testing

At the minimum, data patterns must include a logical (external) checkerboard pattern and its complement, alternating by address and by bit. Actually reading and writing data during the test allows the support circuits to be evaluated as well. A 2-cycle-per-address pattern of read/evaluate –- write the complement of the correct data is preferable to assure each bit is tested equally as a one and a zero.

Recommended tests:

- Expanded range of voltages beyond the normal specified range
- Extended cycle times, encompassing maximum and minimum values
- Other possible variables include temperature, physical data patterns, etc.
- Voltage: nominal +/- tolerance
- Cycle time (refresh time): span at least a factor of 10 higher in frequency or slower in time than the nominal refresh time.

Many chips have good internal voltage regulators and will be insensitive to supply voltage variations. The use of physical data patterns is also highly recommended to provide insight into pattern radiation sensitivities.

3.3.3.5 SRAM testing

Data patterns should include a logical checkerboard, alternating by address and by bit. Recommended variable evaluation includes:

- Extended cycle times encompassing maximum and minimum values
- Voltage: nominal +/- tolerance
- Static and limited dynamic conditions
- Static operation (standby).
- Other possible variables include temperature, physical data patterns, etc.

3.3.3.6 Testing other parts

There are no requirements at this time for soft error test on other classes of parts, such as microprocessors, gate arrays, and other digital product technologies. Appropriate test conditions and interpretation of tests on other classes of parts will be highly dependent on the part function and design. Possible variables include data patterns, voltage, temperature, speed. The test conditions will be highly dependent on the part function.

3.4 Final report

3.4.1 Test data reporting

During the data collection phase of SSER studies for a single device type, the following general information must be recorded:

- Specific type and number of devices tested
- Total duration of the SSER test.
- Effect of different cycle timing or other variables on the test results
- Any indication of latchup or other high-current behavior
- Testing limitations, such as use of test frequencies below maximum rated frequency of operation.

Other information that should be reported includes fail rate estimation technique. The report may also contain fail rates for the different types of fail signatures. Fail signatures can include simple multibit fails, row or column fails, or chip wipeouts, or can be circuit specific (i.e. a latch setting internal logic states, voltages, or redundancy).

3.4.2 Specific items for the final report

In addition to the general guidelines, the specific information that will be included in the SSER final report are:

1) A table showing SSER (in units of kFITs) for each device type. The SSER should be calculated using the methods outlined in Annex A for a specific confidence interval. The confidence interval used must be included. This document does not fix a specific soft failure criterion since customer need defines the acceptable soft error rate. For example, a workstation will require a soft failure rate which is 10-100x lower than a typical mobile phone. Thus the omission of a specific failure rate requirement is intentional – However, the failure measurement technique and data reporting must follow the well-established procedure defined in this document.

2) A detailed description of the physical location of the SSER test system. This should include longitude, latitude, and elevation, as well as building details (i.e., what floor is the tester on, how many floor of concrete above the tester, is the tester located near a window, etc.). Of course it would be desirable to include an estimation of the neutron flux at the tester location, with clear details on how this estimate was made (direct measurement over a particular energy range, based on reference, etc.)

3) Product SSER for standard operating voltages, temperatures, operating frequencies, etc. If on-board ECC is built into the device and active during the tests, this must be clearly specified. For logic and complex circuits, there may be additional issues that alter or mitigate the test vehicle sensitivity, including duty cycle, on-chip ECC, and circuit type.

3.5 Interferences

3.5.1 Introduction

There are several factors that need to be considered in accommodating interferences affecting the SSER test. Each is described herein.

3.5.2 SSER test location

Since a portion of the observed SSER is due to high energy cosmic radiation events, test location can significantly alter the final results. For example, a test run on identical units at two different elevations, longitudes, and latitudes, may exhibit very different SSER. These effects are discussed in greater detail in clause 5.

Another related effect is that of shielding. Although neutrons are relatively hard to shield, the concrete used in most modern buildings does have a shielding effect. So an SSER test run at ground level on the first floor and the same test run in the basement may yield different results. Since there is no simple way to account for all these effects, the location of the test should be well documented, along with comments as to the effective shielding if possible.

3.5.3 Number of errors expected during the SSER test

To perform an SSER test that yields accurate data the test duration needs to be long enough to ensure that the failure rate is within a predetermined confidence interval. In general it is helpful to have some idea of the average SER of the product to be tested. In this way, the sample size and expected test time can be determined ahead of time using chi-squared statistics described in Annex A.

3.5.4 Generalized noise, system errors, and hard failures

To reduce the possible effects of an electrically noisy environment, grounding and shielding techniques must be optimized. The SSER test software and system hardware must be able to discern between a soft error in a device, a system read error during access, and a device hard fail. This is usually achieved by reading the data out several times. If the error persists then it is not a read error and must be a “real” soft error or a hard error. Inverted data (the opposite of what was read out) should then be rewritten to the cell. The cell is then read several times (again to ensure no read errors have occurred). If the data state is correct then the originally observed error can be logged as a soft error. If the data is still erroneous after multiple reads and writes then a hard or intermittent failure has occurred and this device should be removed from the DUT population and replaced with a new device.

4 Accelerated alpha-particle test procedures

4.1 Background

4.1.1 Introduction

The radiation environment of packaged semiconductor devices consists of alpha particles emitted from radioactive impurities in the device materials and cosmic radiation events. Testing for soft errors induced by cosmic radiation is dealt with in clause 5; this section deals strictly with SER induced by alpha particles. Uranium and thorium impurities (U-238, Th-232, and their daughter products) found in trace amounts in the various production and packaging materials emit alpha particles. Alpha particles are strongly ionizing, so those that impinge on the active device create bursts of free electron-hole pairs in the silicon. This free charge can be collected at pn junctions (much like free charge created by light), producing a current spike (noise pulse) in the circuit. These current spikes can be large enough to alter the data state on some circuits. The circuit does not suffer a meaningful level of physical damage, so the circuit still works properly, but the data or instructions within the circuitry may have been corrupted.

The magnitude, shape, and distribution of the noise pulses produced by alpha particles are different from the pulses produced by cosmic ray events. Because of this, the voltage, timing and other fail rate correlations differ for alphas and cosmic rays. In addition, although the cosmic ray flux has a weak dependence on altitude, the alpha flux is independent of altitude, and is only a function of the radioactive impurities present. ***Alpha data can not be used to project cosmic-ray induced fail rates, and cosmic data can not be used to predict alpha-induced fail rates.***

An overall assessment of device's SE sensitivity is complete ONLY when the alpha AND cosmic-ray components have been accounted for.

4.1.2 Guideline

The test method described below defines the requirements and procedures for accelerated SEU/SER testing with alpha particle radiation. Generalized real-time, or unaccelerated**,** testing has been dealt with in clause 3, while accelerated testing for SEU/SER induced by cosmic radiation is dealt with in clause 5.

4.1.3 Limits of test method

The accelerated test method in this section applies ONLY to alpha-particle-induced events. It does NOT apply to terrestrial-cosmic-radiation-induced events or events induced by heavy ions in space or in the upper atmosphere. This test method is designed for the testing of SRAM and DRAM memory arrays~~,~~ but could be adapted to other applications as well.

4 Accelerated alpha-particle test procedures (cont'd)

4.1 Background (cont'd)

4.1.4 Goal of test method

The end product of this accelerated testing is a well-defined estimate of the alpha-particle-induced fail rate for products or circuits using a uniform methodology. The fail rate should be characterized as a function of voltage, timing, and possibly other operating variables. The test method utilizes either, or both, of two types of alpha sources; those simulating uranium/thorium impurities (Th-232, U-238, and their radioactive daughter products) in packaging materials or those simulating emission from lead-based solder compounds (Pb-210 and its daughter products). An acceleration factor is then calculated to account for the test geometry, source flux, and the expected alpha-particle environment in the final packaged part in order to predict the SER rate for the product.

4.1.4 Warnings

These tests may involve hazardous materials, operations, and equipment. Test hardware and parts may become radioactive when recoil fragments or larger fragments of the radioisotope escape the alpha source encapsulation. Good ventilation should be provided as some unsealed alpha sources may emit radon as a decay product. When not in use, alpha sources should be stored away from personnel as some alpha sources also produce low-level gamma radiation. Alpha sources should be handled with care even though alpha emission is not extremely hazardous. It is the responsibility of the user of this test method in consultation with radiation safety personnel to establish the appropriate safety and health practices and to determine the applicability of regulatory limitations

4.2 Test facilities and equipment

4.2.1 Basic test requirement

The basic test requirement for memory arrays is storing a known data pattern in the array while the part is exposed and comparing the stored pattern that is present after the device has been irradiated. At some time during and/or after the exposure, the data is evaluated to identify the number of fails. Other circuits may have different tester requirements and will not be explicitly covered here. The system consists of the input stimulus generator and response recorder that would be designed to accommodate the specified device. Testing requires some sequence of writing data to the DUT, reading the data back, comparing the output data to the written data, and tabulating the number of fails. For simple memory arrays, a bit is failing when the data read from that bit is different from the last data written to that bit. It is also useful to identify failing addresses, and fail times for dynamic tests.

4 Accelerated alpha-particle test procedures (cont’d)

4.2 Test facilities and equipment (cont’d)

4.2.2 DUT holder

The tester setup requires a DUT holder. The DUT holder consists of a DUT card (PC board with a socket or sockets of the appropriate type to accommodate the DUT package type), a DUT card holder, and an interface to the DUT tester. Preferably the DUT card uses zero-insertion-force (ZIF) sockets to minimize the risk of damaging the package pins during insertion and removal of DUTs. While wafer-level probing can be used, it is usually not practicable since it requires valuable prober time to run the tests, and the probe card and probes themselves may not allow proper placement of the alpha source.

4.2.3 Alpha source selection

Two types of alpha sources can be used to simulate the packaged environment: those simulating radiation from uranium/thorium impurities (Th-232, U-238, and their daughter products) or those simulating alpha emission from lead-based solder compounds (Po-210, Pb-210). The preferred sources for determining DUT sensitivity to alpha particles from U/Th impurities are Th-232, Th-228, Ra-226, U-238, etc. (Any isotope that produces a number of different emission energies over the range of 4-9MeV). These should be used for simulating the radiation environment of devices that are essentially encapsulated in molding compound. This is a standard for most “plastic” encapsulation schemes. The preferred sources for determining DUT sensitivity to alpha particles from the Po-210 and Pb-210 impurities in solders are Am-241 or Po-210 (Am-241 is preferred because at 138 days, the half-life of Po-210 is so short that frequent calibration is required). These types of sources should be used when the actual product is packaged in a flip-chip package with solder bumps directly over sensitive device areas.

Pure radioisotope foils or metallic substrate foils with the radioisotopes deposited or diffusion-bonded should be used. A2 or other packaged source configurations should NOT be used since these sources add additional source-to-DUT spacing due to their geometry. In general, solid foils are the best alpha sources since the alpha spectrum will be distributed as it would be in the real device. The foil source area should be much larger than the device area to ensure that nearly all angles of incidence are enabled during irradiation.

The choice of which source to use will be based on many factors, but ultimately, the source should emit alpha particles that are similar to the alpha radiation encountered in the materials in the specific product of interest. It is beyond the scope of this document to describe the means of determining the alpha emissions from materials. However, in any SEU/SER extrapolation based on alpha particles, the assumed package flux or use conditions must be specified. The type, activity, and configuration (type of foil, dimensions, encapsulation layers, etc.) of the source used must also be included with each final report.

4 Accelerated alpha-particle test procedures (cont'd)

4.2 Test facilities and equipment (cont'd)

4.2.4 Test hardware

The test cables should be short enough to allow sufficient test speeds without electrical noise problems in a noisy environment. The tester must be configured to do both static and dynamic testing. The following features are also desirable:

- The ability to adjust and monitor the temperature of the DUT;
- Monitoring current draw to check for latchup;
- Operation at, or near, the rated clock cycle for the DUT (when test is being performed in the dynamic mode).

4.2.5 Test software

The basic requirements for the DUT test system is as follows: 1) Create test conditions for input into the DUT; 2) Identify, record, and correct any errors based on the selected test conditions; 3) Provide good fault coverage. When designing the test system, the experimenter must understand the portion of the die, path, and latch of the device being tested in order to arrive at a quantitative result. The fraction of the time the device is in an SEU/SER susceptible mode and what fraction of the chip's susceptible elements is not tested should be known. Complex devices do not always permit easy testing access. The DUT test system should be capable of:

- controlling device initialization and rudimentary functional checks;
- device operation (dynamic or static operation while under irradiation and device resetting capability);
- error detection and logging.

In addition to possessing the characteristics listed above, the following features are also desirable:

- bit error mapping and data processing, storage and retrieval for display;
- applicability to many device types, e.g., software control with programs written in a high-level language;
- speed of operation and high duty factor (generally, a computer-assisted tester design is implied by this characteristic);
- real-time DUT data display capability providing a higher test throughput and allowing for more precise control of testing;
- data reduction while tests are in progress (this feature is desirable for modification/optimization of test procedures in the light of data being acquired).

4.2 Test facilities and equipment (cont'd)

4.2.5 Test software (cont'd)

The basic test program for memories includes writing a pattern to the device and reading the device periodically during the test. For memories the program should include several different patterns, to ensure that pattern sensitivity is accounted for. The test program for a logic or microprocessor device should include some executions that represent typical operation. The goal of a properly written test program is to ensure that the DUT is operating in a way analogous to the way it will operate in its final product implementation. In general the test program for memories or arrays of latches should include a pattern of ones, zeros, and internal checkerboard, as a minimum, since devices often have a preferred data state which is more robust.

4.3 Testing procedures

4.3.1 Pretest preparations

4.3.1.1 Standard operating procedure

Before beginning irradiation it is important to ensure that all personnel are properly trained on safety issues, and hazard mitigation techniques, that the test equipment has been properly setup, and that the radiation source is operating as expected. Setup conditions vary with each facility.

4.3.1.2 Test plan

A test plan shall be developed to support each test. The test plan will serve as a guide for the procedures and real time decisions to be made during the actual irradiation period. However, no test plan can be followed exclusively, because source/test variables and the results of the earlier runs must be factored into later decisions.

4.3.1.3 Sample selection

Device-to-device variability for soft errors is generally small for devices produced with the same masks and fabrication steps, so a test sample can also be small. However, the system user must be sure that the devices tested are equivalent to actual baseline production devices, because manufacturers often make process/design changes affecting SEU/SER sensitivity without changing the device's numerical designation. In general a minimum requirement to establish a product's alpha particle induced SEU/SER is to test at least two nominal devices each from three different baseline lots.

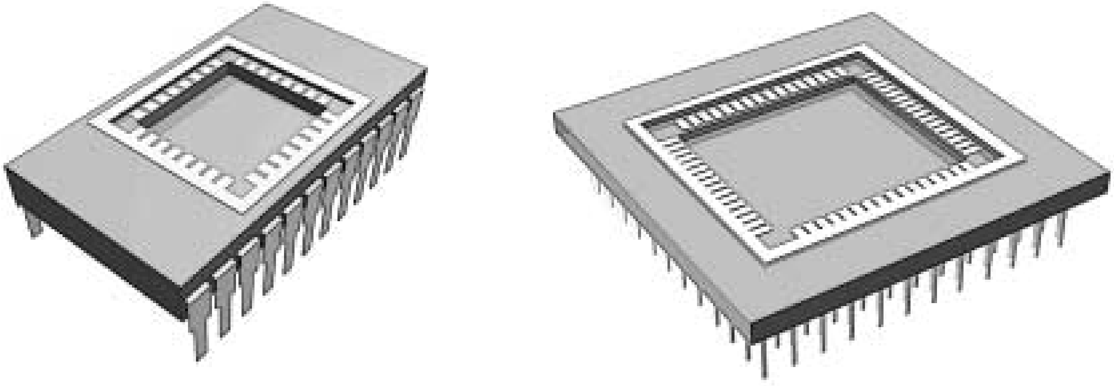
If a special test structure has been designed specifically to mimic a portion of the circuit, this must be specified in the final data sheet. For example if an SRAM is used to determine the SEU/SER sensitivity of an embedded SRAM, this should be noted in the data sheet. Conversely if actual product is used, this should also be noted. If a product is tested which has on-board error-correction codes/circuits (ECC) two tests need to be run, both with ECC enabled and with ECC disabled. If this is not possible, the fact that ECC is present should be included in the data sheet.

4.3 Testing procedures (cont'd)

4.3.1 Pretest preparations (cont'd)

4.3.1.4 DUT preparation

The preferred DUT package is a ceramic dual-in-line package (CERDIP) or pin-grid array package (CERPGA), as illustrated in Figure 4.1a and Figure 4.1b respectively, with the device die mounted and wirebonded within the well or cavity such that the surface of the die is as close as possible to the top surface of the package (this configuration is required to ensure that the alpha source-to-DUT spacing is minimized). Testing of plastic packages is also possible assuming that the plastic encapsulant (mold compound) is etched back to fully expose the chip surface for accelerated testing. Lead-over-Chip (LOC) packages are not suitable since the lead frame shadows a large portion of the device. Flip-chip packages are also not suitable for testing since the bumps shadow most of the die surface. The package type and any modifications should be recorded on the data sheet. If special barrier materials (for example, polyimide, and the like) have been used to coat the chip for alpha particle protection, then this layer should be present during the testing.



a.) **b.)**

Figure 4.1 — Recommended packages for alpha particle testing, a.) ceramic dual-in-line (CERDIP) package, and b.) ceramic pin-grid array (CPGA) package.

4.3.1.5 Source calibration

When performing accelerated alpha SER/SEU testing, the user has the ultimate responsibility for assuring that the alpha source activity is well known and checked as appropriate. Alpha sources lose activity as sputtering (induced by alphas and recoil fragments ejected from the source material) ejects material. Thus at least annual calibration is required to ensure that the source flux is known. The procedure for source calibration is beyond the scope of this document, however some generalized procedures are included in the annex. The type, activity, and configuration (type of foil, dimensions, encapsulation layers, etc.) of the radioisotopic source used must be included in the data sheet.

4.3 Testing procedures (cont'd)

4.3.2 Setup procedure

4.3.2.1 DUT handling

Special care must be taken in handling the DUTs used for accelerated SEU/SER tests because they have been delidded to permit penetration by the alpha particles into the active regions of the device. All parts must be handled with the precautions for parts susceptible to damage from electrostatic discharge. The use of ground planes and straps is highly recommended whenever possible. A standard metal lid for the package should be attached with tape to ensure that the die is protected during handling and storage. The lid is only removed prior to testing with an alpha source.

4.3.2.2 -ATE location

The test equipment should be set up as close to the DUT holder as possible to avoid noise issues related to long cabling. Also ensure that cables are not physically blocking any areas accessed during the replacement of DUTs.

4.3.2.3 Tester check-out

Perform a device tester "dry-run" with the DUT in place prior to running the test with an alpha source. The checkout should be performed with the equipment that will be used to perform the test, including all cables connected as they will be during the irradiation. After any major changes such as replacing the DUT with a non-irradiated device, or changing the cabling arrangement, a dry-run test with no source should be run to verify proper operation of the device and test system. It is important to test the entire system, with the DUT in place, without the source for the same anticipated test time in order to ensure tester integrity.

4.3.2.4 Setup check

Check for correct setup of the equipment by testing each pin of the DUT socket, where applicable. A nonirradiated and well-characterized control part should be inserted in the DUT socket and checked for correct performance without an alpha source. If part performance differs significantly from earlier measurements on this part, check cables, fixtures, etc., and repeat step 4.3.2.3.

4.3 Testing procedures (cont'd)

4.3.2 Setup procedure (cont'd)

4.3.2.5 Alpha source fluence

The total number of alpha particles incident on the DUT must be sufficient to establish with a high statistical confidence that all sensitive volume has been irradiated uniformly. Typically a fluence is used that will induce at least 100 upsets during the test interval. See the annex for discussions on statistically based confidence levels.

First, a run is made with the highest fluence to be used. This is followed by several other runs at lower fluences (e.g., 1/10 the desired fluence) to check for nonlinearities as a function of fluence. If there is fluence dependence (non-linearity), an alpha source with lower flux or shorter test duration should be used. The source flux/test duration should be reduced until the SER vs. fluence data becomes linear. In general however, since the source flux is typically many orders of magnitude higher than the alpha flux in the packaged part, tests at lower fluences are likely to be the most accurate.

4.3.3 DUT testing

4.3.3.1 Load DUT

Remove the nonirradiated control part and place the desired DUT in its socket and run the test program once again to verify proper operation with the new DUT.

4.3.3.2 Load Alpha Source

Place the appropriate alpha source centered over the DUT. The source-to-DUT spacing should be < 1 mm to ensure that the DUT is exposed to alpha particles with virtually all possible angles of incidence. The actual experimental spacing must be recorded on the data sheet. The die should be mounted such that its surface nearly contacts the lid when a lid is attached. Depending on the die thickness and the package well depth, a spacer layer placed between the die and the well bottom maybe necessary to ensure that the die surface is close to the lid surface.

This particular configuration is shown in figure 4.2. Prior to placing the alpha source in position, power down the DUT in order to prevent accidental shorting of the bond wires during source placement. Great care must be used to ensure that the surfaces don't touch, since any contact could short the device and damage the active source encapsulation.

4.3 Testing procedures (cont'd)

4.3.3 DUT testing (cont'd)

4.3.3.2 Load Alpha Source (cont'd)

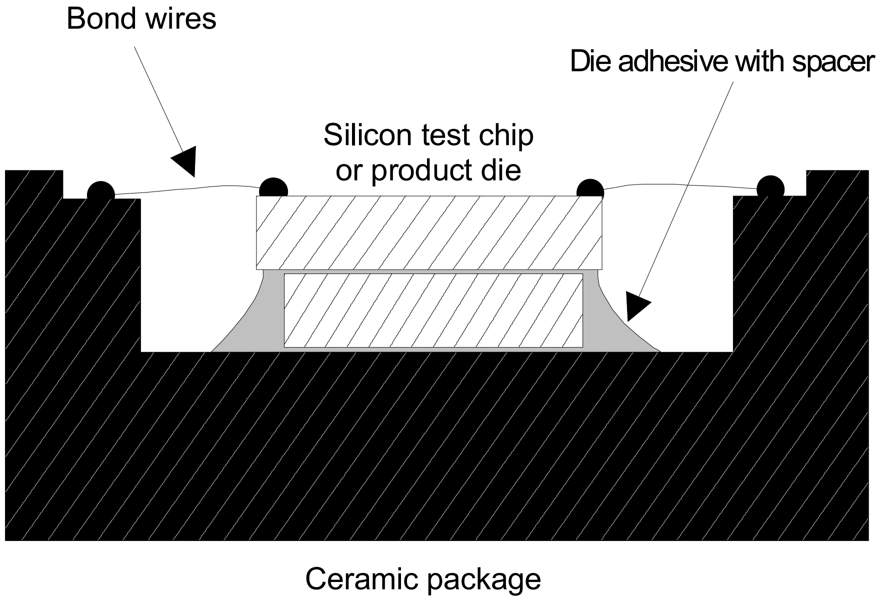


Figure 4.2 — Cross-section through ceramic package illustrating die mounting with spacer to reduce the ultimate source-to-die spacing ensures that the die surface is close to the lid surface.

In addition to being as close to the die as physically possible, the active area of the alpha source should be significantly larger than the DUT. The recommended configuration is shown in figure 4.3.

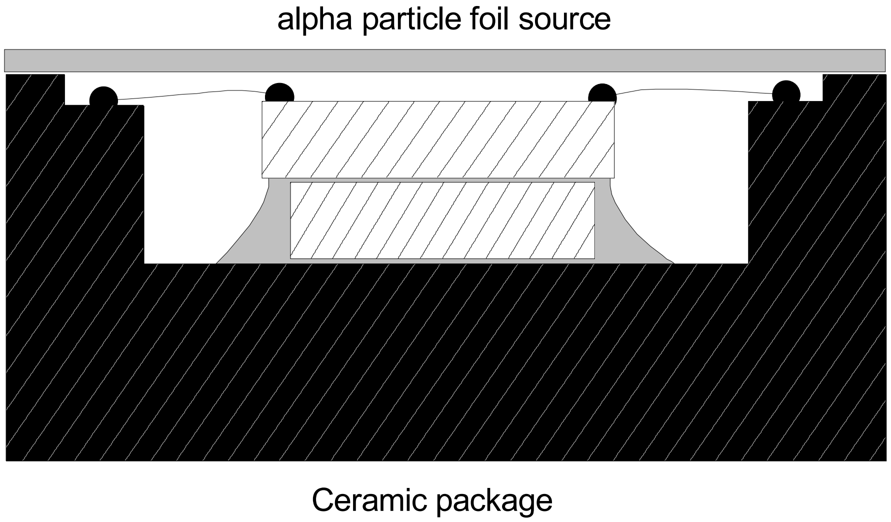


Figure 4.3 — Cross-section through ceramic package illustrating recommended alpha source placement - as close to the die a physically possible.

4.3 Testing procedures (cont'd)

4.3.3 DUT testing (cont'd)

4.3.3.3 General testing specifications

Expose DUT until the desired number of errors (typical more than 100 during the test duration – test statistics are dealt with in detail in the annex) has been measured or the desired maximum fluence has been reached. After extended testing the device should be replaced with a non-irradiated device to ensure aging effects do not affect the results. A minimal test will include:

1) Setup and check out tester with standard part.

2) Load DUT and place alpha source.

3) Initial DUT test

4) Collect data.

5) Final test for part using the same conditions as step 3) to verify consistency of results (this is also an indirect total dose check).

6) Repetition of steps 2) through 5) for additional parts.

For each run, record time, dose, energy, fail count, fail locations, test pattern, voltage, cycle time**,** and DUT identification. Record any problems or unusual behavior. If possible, record the fail signature.

Different circuits will have different impact on the output. For example, a hit on an address decode circuit may cause data to be written to the wrong address, causing two addresses to show up as fails - the address the data was supposed to be written at, and the incorrect address where the data actually was written. Verify the part is being properly operated - e.g., the appropriate address space is being covered for memory parts. Use a source with higher flux if the part is relatively immune to radiation.

4.3.3.4 DRAM testing

At the minimum, data patterns must include a logical checkerboard pattern and its complement, alternating by address and by bit. Actually reading and writing data during the test allows the support circuits to be evaluated as well. A 2-cycle-per-address pattern of read/evaluate –- write the complement of the correct data is preferable to assure each bit is tested equally as a one and a zero.

Required variable evaluations include:

- Voltage: nominal +/- tolerance
- Cycle time (refresh time): span at least a factor of 10 higher in frequency or slower in time than the refresh time.

4.3 Testing procedures (cont’d)

4.3.3 DUT testing (cont’d)

4.3.3.4 DRAM testing (cont’d)

Recommended tests:

- Expanded range of voltages beyond the normal specified range;
- Extended cycle times, encompassing maximum and minimum values;
- Other possible variables including temperature, physical data patterns, and flux.

NOTE Many chips have good internal voltage regulators and will be insensitive to supply voltage variations. Physical data patterns may also provide insight into the ionizing radiation sensitivities of the chip.

4.3.3.5 SRAM testing

Data patterns should include a logical checkerboard, alternating by address and by bit.

Recommended tests include**:**

- Voltage: nominal +/- tolerance
- Static and limited dynamic conditions
- Dynamic tests at maximum rated operating frequency
- Low voltage static operation
- Temperature and flux dependence

NOTE Some TFT and poly load SRAMs have a long cell recovery time after writing and will have measurable fail rate increases at higher cycle times. In addition, there may be support circuit sensitivities that will only appear with dynamic testing.

4.3.3.6 Testing other parts

There are no requirements at this time for soft error test on other classes of parts, such as microprocessors, gate arrays, and other digital product technologies. Appropriate test conditions and interpretation of tests on other classes of parts will be highly dependent on the part function and design. Possible variables include data patterns, voltage, temperature, and speed. The test conditions will be highly dependent on the part function.

4.4 Final report

4.4.1 Test data reporting

During the data collection phase of alpha particle SEU/SER studies for a single device type, the following general information must be recorded:

1) Type of alpha particle source used – isotope (Am-241, Th-232, etc.) and configuration (foil, diffusion bonded, etc.)

2) The source area, source-to-die spacing, alpha particle incident on active die surface, and any other test setup considerations.

3) Type and number of devices tested.

4) Variation of error rates observed for different devices

5) Effect of different cycle timing or other variables on the test results

6) Any indication that latchup or other high-current behavior

7) Testing limitations, such as use of test frequencies below maximum rated frequency of operation.

Other information that should be reported includes fail rate estimation technique. The report may also contain fail rates for the different types of fail signatures. Fail signatures can include simple multibit fails, row or column fails, and chip wipeouts, or can be circuit specific (e.g., a latch setting internal logic states, voltages, or redundancy).

4.4.2 Specific items for the final report

In addition to the general guidelines, the specific information that will be included in the final report are:

1) A plot showing SEU/SER rate vs. Internal Voltage for a range of voltages from the minimum to the maximum specified operating voltage. This plot should include data obtained with a Th-232, U-238, or related source and if applicable (if the product die surface is exposed to alpha particles from solder - as in many flip chip packages), an Am-241 source.

2) A description of the radiation environment assumed in the package. This should be based on direct alpha counting measurements or vendor specifications. The source of the data should be clearly specified.

4.4 Final report (cont'd)

4.4.2 Specific items for the final report (cont'd)

3) Extrapolated product SEU/SER performance. This number should be derived from the product of the expected package flux and the raw SEU/SER data divided by the test flux incident on the package. In the case of SRAMs and DRAMs, the product alpha soft error sensitivity maybe directly determined from this type of testing. If on-board ECC is built into the memory and active during the tests, this must be clearly specified. For logic and complex circuits, there may be additional issues that alter or mitigate the test vehicle sensitivity, including duty cycle, on-chip ECC, and circuit type. The results of the tests and error rate calculation must include the entire range of power supply voltages, along with estimated uncertainty from counting statistics and device variability. Table 4.1 shows a representative format for the final error rate, reported as a FIT rate. Note that depending on the test conditions and part type, there may be more than one such table.

Table 4.1 — Example of Test Summary Data for a 3.3 V DRAM

Vcc (volts)	Extrapolated Alpha Error Rate (FITs)
3.1	$2.6 \pm 0.53 \times 10^2$
3.3	$1.2 \pm 0.34 \times 10^2$
3.45	$8.1 \pm 1.3 \times 10^1$

4.5 Interferences

4.5.1 Introduction

There are several factors that need to be considered in accommodating interferences affecting the test. Each is described herein.

4.5.2 Alpha source calibration

To perform calibration of the alpha source the flux must be reduced to assure that the rate of ion arrival does not impact the measurement. For low flux sources, the source can be placed in close proximity to the detector at atmospheric pressure. At higher intensities that would saturate the detector, the solid angle can be reduced as a means of addressing this problem.

One way to achieve this with high accuracy is the increase the detector-source spacing. However these tests must be performed in a vacuum to ensure that all alpha particles can reach the detector.

The discriminator should be set to ensure that lower energy events are not counted since many of these will be due to non-alpha background radiation. Since alpha energies below 1 MeV do not have the capability to penetrate further than a few microns through most solid materials, it is unlikely that alphas below this energy will contribute to the device SEU/SER and therefore they can be discounted. Setting the discriminator of the detector electronics to cut-off any events below 1 MeV ensures a large reduction in the background. Even with discrimination, the system background level should be ascertained prior to measuring any alpha sources so that the ultimate detection limit and error can be determined.

4.5 Interferences (cont'd)

4.5.3 Number of errors per unit time

To perform an accelerated SEE/SER test, the DUT tester duty cycle must be adequate to handle the flux arriving at the DUT, or the flux must be reduced accordingly. For a memory device for example, only a small percentage of the bits should fail during a test interval, to ensure that multiple events don't flip fails back into a passing mode.

4.5.4 Generalized noise

To reduce the possible effects of an electrically noisy environment, grounding and shielding techniques must be optimized. The DUT must register NO errors for the total test time when no source is present.

4.5.5 Polyimide

If DUTs have a polyimide coating for alpha particle protection that is standard for the packaged product the test must be done with the polyimide present.

If the product is a flip-chip construction with a underflow material, this material must be removed during accelerated testing.

Parts tested with polyimide should also be tested bare to evaluate the effect of the coating.

5 Accelerated terrestrial cosmic ray secondary test procedures

5.1 Background

5.1.1 Introduction

Terrestrial cosmic rays, at sea level up to moderate altitudes, are dominated by neutrons, with some contributions from protons and pions. Neutrons, protons and pions interact with Si nuclei via strong nuclear interactions. These processes, the so-called spallation reactions, produce a variety of secondary particles - protons, neutrons, deuterons, tritons, alpha particles and heavy recoil nuclei like magnesium. The recoil nuclei are strongly ionizing, creating free electron-hole pairs in the silicon. This free charge can be collected at pn junctions (much like free charge created by light), producing a current spike (noise pulse) in the circuit. These current spikes can be large enough to alter the data state on some circuits. The circuit does not suffer a meaningful level of physical damage, so the circuit still works properly, but the data or instructions within the circuitry may have been corrupted.

The magnitude, shape and distribution of the noise pulses produced by cosmic rays are different from the pulses produced by alphas. Because of this, the voltage, timing and other fail rate correlations differ for alphas and cosmic rays. In addition, although the cosmic ray flux has a weak dependence on altitude, the alpha flux is independent of altitude, and is only a function of the radioactive impurities present. ***Alpha data cannot be used to predict cosmic-ray-induced fail rates, and cosmic data cannot be used to predict alpha-induced fail rates.*** An overall assessment of device's sensitivity to SEE (soft error effects) is complete only when the alpha component and the cosmic ray component have been accounted for.

5.1.2 Limits of test method

The test method in this section applies ***only*** to terrestrial-cosmic-ray-induced events, which are dominated by atmospheric neutrons. It does ***not*** apply to alpha-particle-induced events or events induced by heavy ions in space or in the upper atmosphere. This test method is designed for testing memory arrays~~,~~ but could be adapted to other products as well.

5.1.3 Goal of test method

The end product of the test is a well-defined estimate of the terrestrial cosmic ray induced error rate for products or circuits using a uniform methodology. The error rate should be characterized as a function of voltage, timing, and possibly other operating variables. The test method utilizes neutron sources are various energies and/or high-energy proton beams to conduct an accelerated terrestrial cosmic ray error rate measurement.

5 Accelerated terrestrial cosmic ray secondary test procedures (cont'd)

5.1 Background (cont'd)

5.1.4 Warnings

These tests may involve hazardous materials, operations, and equipment. Test hardware and parts may become radioactive when exposed to ion and neutron radiation. It is advisable to visit the test facility during the planning stage to determine the necessary cable length and shielding for the power supplies and control circuits that will be near the test fixture. The expected radiation level of the position should also be determined and sufficient shielding for these complements provided. The length of cable necessary to reach the operator area should also be determined. It is the responsibility of the user of this test method in consultation with radiation safety personnel to establish the appropriate safety and health practices and to determine the applicability of regulatory limitations prior to use.

5.2 Test facilities and equipment

5.2.1 Basic considerations

There is a distribution of neutrons with various energies in the atmosphere. Figure 5.1 shows the nominal distribution at sea level. The purpose of testing devices is to determine how the spectrum of neutron energies will affect the device. Figure 5.1 also shows the energy distribution of the Weapons Neutron Research (WNR) beam (beam line 30 Left) at Los Alamos National Laboratory, which closely matches the neutron spectrum~~,~~ but has much higher intensity. From the Figure 5.1, it is clear that one hour in the WNR beam provides a cosmic ray neutron fluence that is equivalent to about 10^8 hours on the ground in New York City.

It has been pointed out that there may be some error in the intensity measurement of neutrons and there is ongoing work to improve these measurements. Even considering an error the WNR beam is a good match for the typical New York City sea-level neutron flux.

The WNR at Los Alamos is the preferred facility. It can be used in a relatively transparent way to determine the soft error rate from high energy neutrons (> 1 MeV) because its spectrum is so closely matched to the actual terrestrial environment. However, the WNR has limited availability. An alternative way to characterize SEU effects for a chip would be to do a series of experiments using mono-energetic sources at nominal energies of 10-20, 50, 100 and 150 MeV. A continuous cross-section curve $\sigma(E)$ can then be established using these point data.

5.2 Test facilities and equipment (cont'd)

5.2.1 Basic considerations (cont'd)

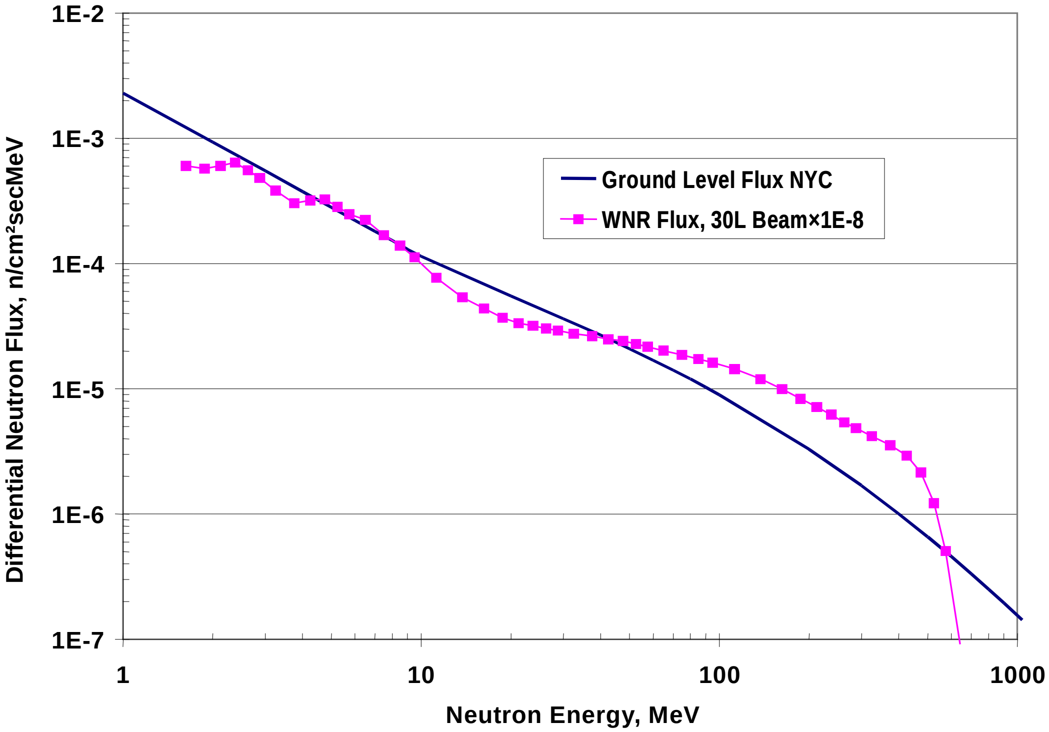


Figure 5.1 — Comparison of Differential Neutron Fluxes, in New York City, and in the WNR 30 Left beam (Reduced by Factor of 1E8) at LANL.

The effect of neutrons on devices depends on the bit failure cross section for soft errors as well as on the distribution of neutron energies. The resulting error rate depends on the integral of the product of the cross section (which is also energy dependent) and the neutron flux. The error rate can be written as:

$$\text{Soft Error Rate} = (\#\ of\ bits) * \int_0^\infty \sigma(E) F(E)\, dE$$

$$\sigma(E) = \frac{\#of\ fails}{(\#neutrons/cm^2) * (\#of\ bits)}$$

where:

σ = bit fail cross-section and F is the differential neutron flux as a function of neutron energy, E.

5.2 Test facilities and equipment (cont'd)

5.2.1 Basic considerations (cont'd)

For energies greater than 50 MeV protons produce reactions in silicon that are very similar to those generated by neutrons. This allows protons facilities, which are generally more readily available, to be used instead of neutron facilities for the higher energy ranges. Figure 5.2 presents published data correlating these sources.

However, it is important to note that protons may produce failure modes that neutrons do not, such as total ionizing dose failure. This is also discussed in section 5.7.2. Observance of effects such as power supply current increases and voltage drifts would be indicative of total ionizing dose effects. If using protons in place of neutrons during testing, the differences between the resulting failure modes must be considered.

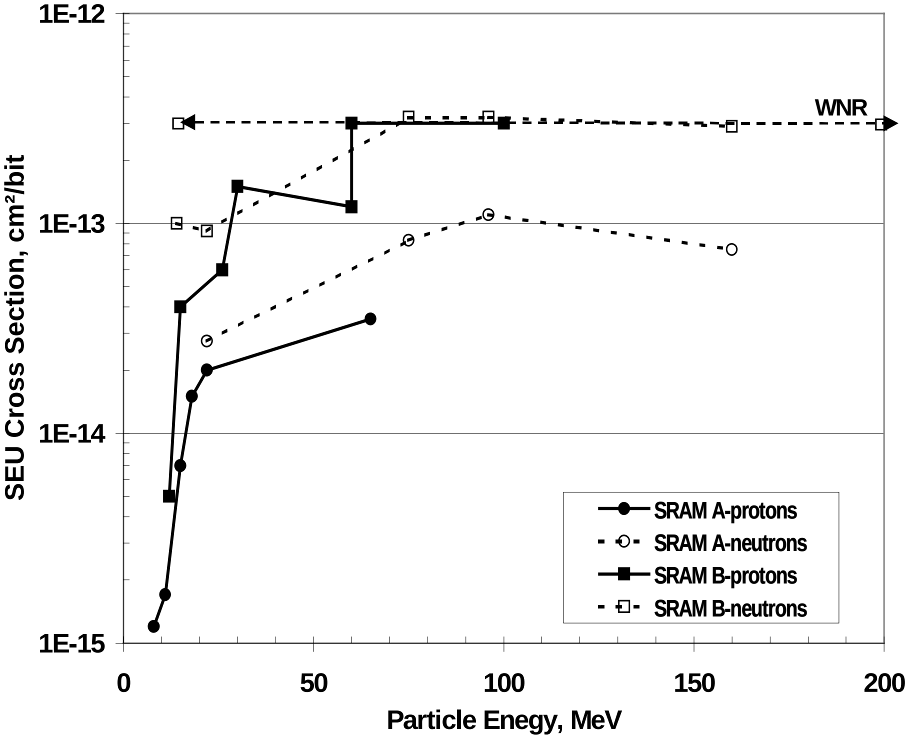


Figure 5.2 — Comparison of the measured neutron and proton SEU cross section as a function of particle energy for two different SRAMs, on a per bit basis.

5.2 Test facilities and equipment (cont'd)

5.2.1 Basic considerations (cont'd)

In some cases, use of low energy neutron beams may be important for determining the SEU effect of the cosmic thermal and epi-thermal neutrons (between thermal and 1 MeV) on devices. This is mainly a concern in low voltage (< 2V) SRAM devices fabricated with high concentrations of ^{10}B. ^{10}B has an extremely high thermal neutron capture cross-section and fissions upon absorbing a neutron. The fission fragments are an alpha particle and a lithium recoil nucleus which are both capable of causing ionization and SEU/SER. However, since the energy of each of the fission fragments is relatively low (< 1.5 MeV) the source of ^{10}B must be in close proximity to the active device silicon (1 um or less). The most common and largest concentration of ^{10}B is in borophosphosilicate glass (BPSG typically contains 5-10% Boron by weight) used throughout the semiconductor industry as a passivation/dielectric layer with improved gettering and lower reflow temperatures. Another source is BF-based implants because the mass separation is not as efficient as direct ^{11}B implantation.

To account for the thermal/epi-thermal activation of ^{10}B devices should be exposed to cold or thermal neutron beams. For comparative purposes and radiation lot acceptance testing, single-energy laboratory sources (14 MeV for instance) may also be used provided that a correlation has been previously established with more rigorous testing at several energies. Data obtained with single-energy sources may suitable for comparisons of different designs or geometries, or parametric studies of upset rates, but are not an acceptable substitute for more rigorous testing over a range of energies that is required by the standard.

5.2.2 Facilities for SEU Studies/Beam Characteristics

Very few mono-energetic neutron facilities are available. In actual practice, one often uses both proton and neutron beams. A list of proton and neutron facilities is listed in Annex D.

5.3 Equipment - tester

5.3.1 Basic test methodology

The basic test methodology for memory arrays is storing a known data pattern in the array while the part is exposed and comparing the stored pattern that is present after the device has been irradiated. At some time during and/or after the exposure, the data is evaluated to identify the number of errors. Other circuits may have different tester requirements and will not be explicitly covered here.

The system consists of the input stimulus generator and response recorder that would be designed to accommodate the specified device. Testing requires some sequence of writing data to the DUT, reading the data back, comparing the output data to the written data, and tabulating the number of errors. For simple memory arrays, a bit is failing when the data read from that bit is different from the last data written to that bit. It is also useful to identify failing addresses, and time of failure for dynamic tests.

5.3 Equipment – tester (cont'd)

5.3.2 DUT holder

The tester set-up requires an adjustable DUT holder. The DUT is a packaged part. Delidding is not required. Probed parts are not practicable since they require valuable beam time to make good contact, require tilting of the probe station to accommodate horizontal beams, and are difficult to transport.

A typical DUT holder consists of a tripod supporting a card with a socket for the part. The tripod may also support an connector, allowing a card assembly (like a DIMM -- dual inline memory module) to be tested. The cable from the DUT to the tester must be long enough to allow the tester to be located outside the beam path, and also to allow flexibility of location in facilities with limited free space. Cabling is unique to the test facility and should be determined by a pre-test visit.

5.3.3 Test hardware

Beam facilities currently do not provide microelectronic test equipment; thus the test setup must be portable so the user can transport it to the facility. The ATE (automatic test equipment) must also be able to tolerate levels of stray radiation and possibly poor quality electrical power. The test cables should be short enough to allow sufficient test speeds without electrical noise problems in a noisy environment.

The ATE controller is frequently located some distance from the ATE, allowing the user to operate the tester from behind appropriate shielding.

It is important to check the physical dimensions, accessibility, and power availability at the beam facility before making the trip. The ATE should also be able to stand up to shipping (to the beam site) and to be reassembled at the beam site in reasonable time. The ATE must be configured to do both static and dynamic testing.

In addition to possessing the characteristics listed above, the following features are also desirable:

1) the ability to adjust and monitor the temperature of the DUT;

2) monitoring current draw to check for latchup;

3) operation at, or near, the rated clock speed for the DUT (when test is being performed in the dynamic mode).

5.3 Equipment – tester (cont'd)

5.3.4 Test software

The basic requirements for the DUT test system are as follows:

1) Create test conditions for input into the DUT.

2) Identify, record**,** and correct any errors based on the selected test conditions.

3) Provide good fault coverage.

When designing the test system, the experimenter should understand the portions of the die, signal path, and latching circuits of the device being tested in order to arrive at a quantitative result.

The fraction of the time the device is in a SEE susceptible mode and what fraction of the chip's susceptible elements is not tested should be known. Complex devices do not always permit easy testing access.

The ATE should be capable of

1) Controlling device initialization and rudimentary functional checks;

2) Device operation (dynamic or static operation while under irradiation and device resetting capability); and

3) Error detection and logging.

In addition to possessing the characteristics listed above, the following features are also desirable:

1) Bit error mapping and data processing, storage and retrieval for display.

2) Applicability to many device types, e.g., software control with programs written in a high-level language.

3) High speed operation and high duty factor. Generally, a computer-assisted ATE design is implied by this characteristic.

4) Real-time DUT data display capability providing a higher test throughput and allowing for more precise control of testing.

5) Data reduction while the test in progress. This feature is desirable for modification/optimization of test procedures in the light of data being acquired.

5.4 Test plan

5.4.1 Basic procedures and facility selection

A test plan shall be developed to support each test. The test plan will serve as a guide for the procedures and real time decisions to be made during the actual irradiation period. However, no test plan can be followed exclusively, because source/test variables and the results of the earlier runs must be factored into later decisions. Common practice is to do tests with the beam at normal incidence. In most cases there is no angle dependence, allowing tests to be done at other angles. A cursory check of angle dependence is recommended.

A “reference chip” with a relatively high soft error rate that is capable of withstanding a relatively high total dose level is recommended as part of the testing approach. Normal practice will be to do tests on the “reference chip” before each test series in order to provide validation of the test equipment and a secondary means of calibrating the facility. After the “reference chip” is selected, it should be tested multiple times to establish the consistency and variability of the measured SER.

For each part, the initial test shall be repeated at the end of a sequence of tests. If the second set of tests do not agree with the initial set, then additional testing must be done to determine whether radiation damage (total dose; see 5.4.2.4) or other testing issues is responsible for the difference in results. Interpretation of these results must take the normal variation expected for such testing into account.

A minimal test plan would include:

1) Set-up and check-out tester;

2) Initial beam and setup check using 'golden' part;

3) Initial test for part;

4) Data collection;

5) Final test for part using the same conditions as step 3) to verify consistency of results (this is also an indirect total dose check);

6) Repeat steps 3) through 5) for additional parts;

7) Final beam and set-up check ('golden' part).

5.4 Test plan (cont'd)

5.4.2 Test conditions

Because of the need to use portable ATE (automatic test equipment) for radiation test systems, a more limited set of dynamic tests is specified in the minimum test requirements.

5.4.2.1 DRAM

At the minimum, data patterns must include a logical checkerboard pattern and its complement, alternating by address and by bit.

Actually reading and writing data during the test allows the support circuits to be evaluated as well. A two-cycle-per-address pattern of read/evaluate –- write the complement of the correct data is preferable to assure each bit is tested equally as a one and a zero.

Required variable evaluations include:

- voltage: nominal +/- tolerance
- cycle time (refresh time): span at least a factor of 10 higher in frequency or slower in time than the refresh time.

Recommended tests:

- Expanded range of voltages beyond the normal specified range
- Extended cycle times, encompassing maximum and minimum values
- Other possible variables, including temperature, physical data patterns, and flux.

NOTE Many chips have good internal voltage regulators and will be insensitive to supply voltage variations. Physical data patterns may also provide insight into the ionizing radiation sensitivities of the chip.

5.4.2.2 SRAM

Data patterns should include a logical checkerboard, alternating by address and by bit.

Required variable evaluation includes:

- voltage: nominal +/- tolerance
- static and limited dynamic conditions

Recommended tests include:

- Dynamic tests at maximum rated operating frequency
- Low voltage static operation
- Temperature and flux dependence

5.4 Test plan (cont'd)

5.4.2 Test conditions (cont'd)

5.4.2.3 Other parts

This document does not address soft error tests on other classes of parts, such as microprocessors, gate arrays and other digital part technologies.

Appropriate test conditions and interpretation of tests on other classes of parts will be highly dependent on the part function and design. Possible variables include data patterns, voltage, temperature, and speed. The test conditions will be highly dependent on the part function.

5.4.2.4 Total dose problems

Some parts may suffer total dose damage. This damage may show up as a hard fail that is not fixed by resetting the part or as parametric degradation. Parametric degradation can affect the soft error rate and is also an indication that the dose is approaching the level where significant damage is starting to occur.

Some total dose effects may disappear with time (days or months) as the damage is allowed to anneal. For these parts, a greater number of tests and higher doses will result in erroneously high failure rates. The typical dose that a part is subjected to in a beam is many times greater than the total dose the part would be exposed to in normal terrestrial operation .

It may be necessary to reduce the target number of failures and/or split up the tests over more parts. If the testing is split between additional parts, it is still important to run a baseline (nominal conditions) test on each part as the first and last test for each part.

5.4.3 Sample selection for process characterization

A minimum of 2 samples each from 3 lots should be tested to investigate process variation.

5.5 Testing procedure

5.5.1 ATE Setup and Check

The ATE should not be located in the path of the beam. Scattered radiation near the beam may also affect test equipment. Allowable equipment locations depend on the particular facility.

After setting up the ATE, a “reference” part (defined previously in 5.4.1) should be tested in the beam. It is preferable to use the same part for every test session. This part should be tested at the beginning and end of every test session to assure beam and tester consistency.

5.5 Testing procedure (cont'd)

5.5.2 Beam parameters

5.5.2.1 Beam check

Most facilities provide beam calibration. In most cases users will rely on calibration and beam uniformity at the facility.

In cases where facility calibration is not well established, then it will be necessary to measure the flux, energy and spatial uniformity (area) of the beam. Details vary with facility~~,~~ and are the beyond the scope of this document.

5.5.2.2 Beam fluence

The total number of particles must be sufficient to establish with a high statistical confidence that all sensitive volume on the DUT have been irradiated. A minimum fluence is used that will induce a minimum of 100 upsets during the test interval. See the Annex C for discussions on statistically based confidence levels.

5.5.2.3 Beam flux

Typically, start with the highest flux. If the fail rate is too high (> about one per second), the flux should be dropped. It is preferable to also run at a lower flux (e.g., 1/10 normal flux) to check for a nonlinear SER flux dependence.

If there is a nonlinear flux dependence, the flux should be dropped until the flux dependence becomes linear. The beam flux is many orders of magnitude higher than the flux at use conditions; thus the lower flux measurements would be the most useful.

If high-energy protons or monoenergetic neutrons are used, then three different energies should be used at approximately 50, 100 and 150 MeV (the exact values depend somewhat on the test facility).

When protons are used instead of neutrons, it is also necessary to do tests with neutrons with energies in the range of 10-20 MeV.

5.5.3 Operating procedure - data collection

5.5.3.1 DUT/ATE check

After setting up the ATE, perform all of the test runs on all parts with the beam off to assure there are no other sources of soft failures. This may be done before, between or after the actual test runs.

5.5 Testing procedure (cont'd)

5.5.3 Operating procedure - data collection (cont'd)

5.5.3.2 Static vs. dynamic testing

For static tests, testing and data collection occurs after the test run is completed, comparing each bit with the expected value.

For dynamic tests, the preferred way is to do data collection during the time that the beam is striking the device, writing complementary patterns after each cycle. It is also possible to do functional testing after the run is completed, but that approach limits the ability to determine which point in the cycle that the observed errors occurred.

The first test should be at nominal operating conditions. After completing all conditions in the test plan (and any new conditions based on the test results), repeat the first test for the DUT to assure no problems with total dose, beam consistency, etc.

5.5.3.3 Data Collection Requirements

For each run, record time, dose, and energy, upset count, upset locations, test pattern, voltage, cycle time and DUT identification. Record any problems or unusual behavior.

If possible, record the upset signature. Different circuits will have different impact on the output. For example, a hit on an address decode circuit may cause data to be written to the wrong address, causing two addresses to show up as fails - the address the data was supposed to be written at, and the incorrect address where the data actually was written.

Verify the part is being properly operated, i.e., the appropriate address space is being covered for memory parts. Verify that the part is in the beam. Recheck the beam/ATE with a similar control part known to fail. Increase the flux; perhaps the part is relatively immune to radiation.

5.6 Final report

5.6.1 Variation of cosmic rays with altitude and geomagnetic latitude

The neutron spectrum depends on altitude and latitude. This procedure requires the use of the spectrum at New York City in calculating failure rates. Annex E shows how to adjust the error rates calculated for the NYC spectrum for other locations.

5.6 Final report (cont'd)

5.6.2 Failure rate estimation from accelerated testing at WNR

Since the WNR neutron beam has a neutron energy spectrum very similar to that of the terrestrial neutron energy spectrum, the per bit upset cross-section obtained at WNR can be used directly to estimate the terrestrial failure rate.

The per bit SEU failure cross-section due to the entire WNR energy spectrum is given by:

$$\sigma = \frac{(\#\ of\ errors)}{(\#\ of\ neutrons / cm^2) * (\#\ of\ bits)}$$

The terrestrial differential neutron flux in New York City is given in Figure 4.1 in graphical form, and in tabular form in Annex D. When integrated over the energy range of 10-10000 MeV, the neutron flux is 3.9×10^{-3} n/cm²s or 14 n/cm²h. In the terrestrial neutron environment, the neutron flux in the 1 - 10 MeV range, 4.0×10^{-3} n/cm²s (or 14.4 n/cm²h) is almost identical to the integral flux of all of the neutrons with energies above 10 MeV.

Neutrons with energies less than 10 MeV have traditionally produced very few additional upsets compared to the higher energy neutrons and so can be ignored. Thus, the terrestrial failure rate is estimated to be:

$$SER = 14 \times \sigma \times \#\ bits\ (upset/h)$$

It is important to note that for devices with significant SER sensitivity to the less than 10 MeV range, the assumption of a 10 MeV cuttoff is not appropriate.

For locations other than New York City, Annex D provides details of how the NYC flux can be modified to yield the terrestrial neutron flux at these other sites. Thus for other locations, the appropriate terrestrial neutron flux for energies > 10 MeV will be a value different than 14 n/cm²h.

5.6.3 Failure rate estimation from accelerated testing at monoenergetic sources

5.6.3.1 Cross section

Determine the bit fail cross section for each energy (nominally 14, 50, 100 and 150 MeV). Assume that the measured proton cross section at 150 MeV applies at energies above 150 MeV (the asymptotic nature of the cross section with energy has been verified through measurements by numerous researchers), and extrapolate that cross section to an energy of 2 GeV (only 1% of the neutrons > 10 MeV are above 2 GeV). If device cross-section at 14 MeV is orders of magnitude less than at 50 MeV, one can assume a cutoff of 10 MeV.

5.6 Final report (cont'd)

5.6.3 Failure rate estimation from accelerated testing at monoenergetic sources (cont'd)

5.6.3.2 Numerical Integration of Cross Section and NYC Neutron Spectrum

Integrate the cross section obtained in the previous subsection over energies from the cutoff energy (10 MeV) to 2 GeV. Using the atmospheric neutron environment of Figure 5.1 (Annex D, Table D.1) and the energies recommended, the SER rate is:

> SER = (# of Bits) x [(3.93 x σ(150 MeV)) + (1.83 x σ(100 MeV)) + (3.72 x σ(50 MeV) +(3.86 x σ(14 MeV))]

Convert the result to FITs by multiplying the upset rate (upsets/hour) by $1\text{x}10^9$.

5.6.4 Test data report

The results of the tests and error rate calculation must include the entire range of power supply voltages, along with estimated uncertainty from counting statistics and device variability. Table 5.1 shows a representative format for the final error rate, reported as a FIT rate at sea level in NYC. Note that depending on the test conditions and part type, there may be more than one such table.

Table 5.1 — Example of Test Summary Data for a 3.3 V DRAM

Vcc (volts)	Error Rate at Sea Level (FITs)
3.15	$2.6 \pm 0.53 \times 10^2$
3.3	$1.2 \pm 0.34 \times 10^2$
3.45	$8.1 \pm 1.3 \times 10^1$

Additional data required for the report includes the following:

1) Specify whether the WNR or discrete energy approach was used

2) For the discrete energy approach, indicate which energies were used

3) Number of devices tested

4) Variation of error rates observed for different devices

5) Effect of different cycle timing or other variables on the test results

6) A table showing the number of upsets or errors at each energy

7) Any indication that latchup or other high-current behavior was observed

8) Testing limitations, such as use of frequencies below maximum rated specification limit.

5.6 Final report (cont'd)

5.6.4 Test data report (cont'd)

Other information that should be reported includes fail rate estimation technique. The report may also contain failure rates for the different types of fail signatures. Fail signatures can include simple multibit failures, row or column failures, total chip failures, or can be circuit specific (e.g., a latch setting internal logic states, voltages, or redundancy).

5.7 Interferences

5.7.1 Beam Flux

In normal use, cosmic particle impingements will be separated by significant lengths of time. It is possible the high flux associated with accelerated testing can produced abnormally high fail rates.

Parts with high sensitivity may suffer fails induced by a high proton flux. In addition, a very high flux (proton or neutron) beam may induce extra fails in parts with slow recovery times. To check for this problem, parts should be evaluated at two different fluxes, where possible. However, that is not possible at the WNR facility.

If the fail rate is the same with the two flux conditions, there is no problem. If the fail rate (per particle) drops with the lower flux, then lower fluxes yet should be evaluated until the fail rate stabilizes. If the fail rate increases at a lower flux, the ATE should be evaluated to assure it could record fails fast enough.

5.7.2 Total dose damage

Total dose effects are evaluated by subjecting parts to the same test conditions for the first and last tests they receive. If the fail rates are the same, the total dose effects should not be affecting the results, although total dose effects may only show up under certain test conditions (e.g., low fail rate conditions). The total dose can be estimated from Table 5.2.

Table 5.2 — Total Dose for Various Proton Energies

Proton Energy (MeV)	**Total Dose from 1 x 10^{10} p/cm^2 [rad(Si)]**
50	1590
100	880
150	600

5.7 Interferences (cont'd)

5.7.3 Package Shadowing

Shadowing is unlikely to be a problem with neutron beams. Proton beams are attenuated through normal packaging materials, but a total thickness of packaging less than 3 mm thick in front of the semiconductor surface will not attenuate the beam significantly. Any additional shielding present (greater than 3 mm) should be noted in the final report.

5.7.4 Latchup

In some parts, the current pulse associated with the ionizing radiation can induce latchup. Since the high currents associated with latchup may damage the part, it should be checked thoroughly before continuing with additional testing to ascertain the additional test data will be valid. The observed latchup rate should be reported in the final report.

5.7.5 Noise

Running tests with the part in the test location with the beam *off* will assure the part/tester is not suffering from other noise/interference problems. It is also useful to test parts with the part physically moved out of the beam, but with the ATE in the same location as for beam testing and with the beam *on* to check for effects of stray radiation on the ATE .

Annex A -- SSER Statistics (Informative)

A.1 SSER testing

In typical life testing a random sample of N units is placed on test under some specified set of operating conditions, and the number of failures and time of occurrence is recorded. In the SSER test, N devices are placed on test under normal (unaccelerated) operating conditions (voltage, temperature, operating frequency) and the number, location, and time of each soft failure is recorded. Since soft errors are not permanent (eliminated when new data is written) this test can be thought of as a life-test with replacement (in which a failing device is replaced with a new device). Note that unlike standard life testing, in SSER testing, it is the number of failures, ***not*** the lifetime, that is the random variable.

Since the SSER test deals with many devices over long periods of time, the concept of device-hours is often used. This is simply the product of the number of devices and the total test time in hours. It should be noted that device-hours assumes a relatively large number of devices and long test times. Thus a 1000 DUT test run for 1000 hours is equivalent to 1,000,000 device-hours. Running 2000 or 3000 devices for 500 or 250 hours should give similar results, but running 1 DUT for 1,000,000 hours or 1,000,000 DUTs for 1 hours will probably yield very different results. Thus it is assumed that a typical SSER test the number of devices and test hours will be within the same range.

A.2 Designing an SSER Experiment

Suppose we had on hand 2000 nominal devices and we wanted to determine with 95% confidence level whether they were at or below a certain SER level and we had some understanding of what the mean SER should be (from accelerated SER studies). How long would we have to test? To answer this question we use one-side (we are only concerned with ensuring that the product's SER is always ***below*** a specified level) of the confidence interval defined by chi-squared statistics. An approximate confidence interval for this type of problem is shown in equation 1.

$$\frac{2T}{\chi^2_{2k+2}} < \mu < \frac{2T}{\chi^2_{2k}} \qquad (1)$$

where T is device-hours, μ is the mean time to fail, and the subscripts on the χ^2 represent the degrees of freedom and k is the soft number of failures during the test. Since we are interested in the soft failure rate that is the reciprocal of the time-to-fail (1/T), equation 2 is recast as follows:

$$\frac{\chi^2_{2k}}{2T} < \frac{1}{\mu} < \frac{\chi^2_{2k+2}}{2T} \qquad (2)$$

Annex A -- SSER Statistics (Informative) (cont'd)

A.2 Designing an SSER Experiment (cont'd)

Since we are only interested in ensuring that the average SER is below a certain specified value, only one side of the interval in equation 2 is used:

$$SSER < \frac{\chi^2_{2k+2}}{2T} \qquad (3)$$

In Table A.1, k is the number of errors and 2k+2 is the degrees of freedom. The next column includes the chi-squared values for 95% confidence intervals. The last 4 columns list the test time required (in device-hours) to achieve a given number of errors assuming a 95% confidence level for a specific mean SER of μ.

Table A.1 — Device-hours required for 95% confidence levels for various mean SER.

k	*2k+2*	$\chi^2_{(1-0.05)}$	μ =50 FITs	μ =500 FITs	μ =5 kFITs	μ =50 kFITs
0	2	5.991	59914764	5991476	599148	59915
1	4	9.488	94877285	9487728	948773	94877
2	6	12.592	125915774	12591577	1259158	125916
3	8	15.507	155073125	15507312	1550731	155073
4	10	18.307	183070290	18307029	1830703	183070
5	12	21.026	210260554	21026055	2102606	210261
6	14	23.685	236847823	23684782	2368478	236848

Hence, if we wanted to verify to 95% confidence the SER of a part thought to have a mean SER of 5000 FITs (as estimated by ASER testing) and we wanted to observe at least 4 soft errors (to be sure these devices fail at all), we would need to test for 1,830,703 device-hours (k=4 errors and μ=5000 FITs). Assuming we had a SSER test capacity of 2000 DUTs this would lead to a total test time of 915 hours (~38 days) on average. Table A.1 can be generated for other confidence intervals (60%, 99%, etc.), and, as expected, increasing the confidence level increases the test time required. In general it is best to design experiments in which several failures are observed before the completion of the test. If a test is done where no errors are observed, one can only say that the SSER is below a certain failure rate but cannot say how much below.

Annex B - Equipment (normative)

B.1 Radiation sources and test apparatus

B.1.1 Radiation sources

The radioisotope sources to be used come in a wide variety or form factors and isotopes that define their energy distribution, intensity, and applicability to simulating SEE/SER. The typical configuration is a metal substrate on which a radioisotope has been deposited and diffusion-bonded by annealing or a solid radioisotope foil. A2 capsules should not be used as their configuration introduces additional source-to-die spacing that is undesirable.

B.1.2 System characteristics

This test method is limited to use with radioisotopic alpha particle sources. In addition to supplying a calibrated alpha source whose active area is larger than the DUT, the test facility and/or user must also provide a method to ensure that the source-to-die spacing is < 1 mm. The final source-to-die spacing should be recorded.

B.2 Test instrumentation

DUT test system. The system consists of the input stimulus generator and response recorder, which would be designed to accommodate the specified device.

B.2.1 DUT test system

The test board serves two purposes: first, it provides a stable mechanical interface to the test stage and second, provides electrical interconnection between the DUT and the external support equipment. The test board/socket must be capable of positioning each DUT within 1 mm of the alpha source.

B.2.1.1 Test modes

Both ac (dynamic) and dc (static) test modes are desired. Dynamic testing assures that input stimulus and circuit changes are coincident demonstrating failure modes that would only be apparent under these conditions (e.g., write failures in SRAMs). Static mode testing is desirable since some circuits are more sensitive after circuit relaxation has occurred (e.g., DRAM discharges during static conditions). It is also easier to ascertain transients during a static test since the output state can be monitored continuously.

B.2 Test instrumentation (cont'd)

B.2.1 DUT test system (cont'd)

B.2.1.2 Basic requirements

The basic requirements for the DUT test system are as follows:

1) Create test conditions for input into the DUT;
2) Identify, record and correct any errors based on the selected test conditions;
3) Fault coverage. When designing the test system, the experimenter must understand the portion of the die, path and latch of the device being tested in order to arrive at a quantitative result. The fraction of the time the device is in an SEE/SER susceptible mode and what fraction of the chip's susceptible elements is not tested should be known. Complex devices do not always permit easy testing access.

B.2.1.3 Basic capabilities

The DUT test system should be capable of:

1) Controlling device initialization and rudimentary functional checks;
2) Device operation (dynamic or static operation while under irradiation and device resetting capability);
3) Error detection and logging;
4) Operation at, or near, the rated clock cycle for the DUT (when test is being performed in the dynamic mode);
5) Known duty factor (ratio of device "sensitive" time to total elapsed time). Knowledge of the duty factor is required to quantify device vulnerability.

B.2.1.4 Additional capabilities

In addition to possessing the characteristics listed in 4.2.2.3, the following features are also desirable:

1) Bit error mapping and data processing, storage and retrieval for display;
2) The ability to adjust and monitor the temperature of the DUT;
3) Applicability to many device types, e.g., software control with programs written in a high-level language;
4) Speed of operation and high duty factor. Generally, a computer-assisted tester design is implied by this characteristic;
5) Real-time DUT data display capability providing a higher test throughput and allowing for more precise control of testing;
6) Data reduction while tests is in progress. This feature is desirable for modification/optimization of test procedures in the light of data being acquired.

B.3 Alpha detection and counting

B.3.1 Surface barrier detector

A silicon surface barrier detector can be used to measure the alpha source activity and energy. Detector systems require that there be an adequate time period between hits, known as the "dead time", for the system to recover. If an ion hits the detector during this time period it will not be correctly counted. To assure that this condition does not occur, choose the appropriate aperture size for the various flux rates. A typical aperture size would be 0.1 cm^2, for a flux range from 10^3 to 10^6 ions/cm^2xs. Increasing source to detector spacing can also be used to ensure that the system dead-time requirement is met. The source is placed a measured distance from the detector to reduce the effective flux reaching the detector (since the detector subtends a smaller solid angle).

B.3.2 How the durface barrier detector works

The surface barrier detector is basically a diode with a large depletion region, which can collect the electron-hole pairs that are created in the material by the impinging ions. The number of electron-hole pairs that are created in the silicon is a function only of the initial energy of the ion hitting the detector. Almost all of the ion's original energy will be given up in this manner. The remaining energy is transferred into crystal lattice damage, but this will only be a small fraction of the total energy. The spatial distribution of created electron-hole pairs, will be a function of the ion species. For this reason, it is important that the depletion region of the surface barrier detector be larger than the range of the ion/energy of interest. The beam flux should be sufficiently low to avoid pile up. How much of the beam is scattered and the peak energy position indicates whether or not the desired ion species is present.

B.3.3 Degradation of the surface barrier detector

Lattice damage builds up over the lifetime of a surface barrier detector. Damage to the lattice degrades the efficiency of charge collection. In addition, corrections for the charge that is deposited in a dead layer or the entrance window must be made. In order to account for charge collection efficiency, the detector must be calibrated before use. This calibration is achieved by exposing the detector to an alpha particle source of a known energy. The alpha particle source is typically americium-214 (Am), which is mounted on the detector shutter typically about 4 cm from the detector surface.

Annex C - Counting statistics (informative)

C.1 Standard deviation

Low probability events, such as the case where a small fraction of incident particles from a radioactive source or accelerator beam produce a measurable event, can be described by the Poisson distribution. For a Poisson distribution the standard deviation, σ, depends on the number of events that are observed. If N events occur, the standard deviation is given by

$$\sigma = 1/\sqrt{N} \tag{1}$$

Thus, at least 100 events must be observed in order to keep the standard deviation at 10% or less. Note that this relationship only considers the statistical properties of a process described by an ideal Poisson distribution, and does not take other experimental uncertainties into account. It is common practice to use “error bars” in plotting data from counting experiments that reflect the standard deviation from counting statistics.

C.2 Estimating probability for results with low numbers of observed events

There are cases of interest where small numbers of events are observed (including the case where no events occur) when a large number of particles (P_N) are incident on the device. The cross section can be bounded for such cases using the upper and lower counting events in the table below. Values are given for 1% and 5% confidence limits. In using this table, the first column is the actual number of events observed in the experiment. The upper and lower limits show how high (or low) the number of events could actually be if the experiment were continued for much longer time periods. The probability that the number of counts exceeds the upper limit is 1% for the 99% confidence limit and 5% for the 95% confidence limit.

	Confidence Limit			
Total No. of events observed	**99%**		**95%**	
	Lower Limit	**Upper Limit**	**Lower Limit**	**Upper Limit**
0	0.0	5.3	0.0	3.7
1	0.0	7.4	0.1	5.6
2	0.1	9.3	0.2	7.2
3	0.3	11.0	0.6	8.8
4	0.6	12.6	1.0	10.2
5	1.0	14.1	1.6	11.7
6	1.5	15.6	2.2	13.1
7	2.0	17.1	2.8	14.4
8	2.5	18.5	3.4	15.8
9	3.1	20.0	4.0	17.1
10	3.7	21.3	4.7	18.4
20	10.4	34.7	12.2	30.9
50	33.7	71.3	37.1	65.9
100	76.1	128.8	81.4	121.6

Annex D – Neutron and Proton Test Facilities (informative)

Listed in Table D.1, are the major accelerator facilities in North America, which support on-going SEU programs for outside user groups. Two remarks are in order:

1) All facilities listed below use monoenergetic and quasi-monoenergetic beams. Los Alamos National Laboratory has a continuous high-energy neutron beam that has an energy spectrum very similar to atmospheric neutrons.

2) The Northeastern Proton Therapy Center in Boston is planned to be in operation in the middle of 2000. After that, the Harvard Cyclotron will be phased out and closed. At the time of writing this report, however, the prospects of doing SEU work at the new facility are not completely clear.

Table D.1 — Facilities for SEU Studies in North America

Institution	Beam Type	Energy Range	Type of Work
Harvard Cyclotron	Proton	160 MeV	Radiation therapy Applied research SEU
North Eastern Proton Therapy Center	Proton	200 MeV	Radiation therapy SEU
Indiana University Cyclotron Facility	Proton	160 MeV	Basic nuclear research
	Neutron	160 MeV	Radiation therapy SEU
Los Alamos National Laboratory	Proton	800 MeV	Basic nuclear research
	Neutron	800 MeV	Applied research SEU
Crocker Nuclear Lab. at UC Davis	Proton	67.5 MeV	Applied research
	Neutron	65 MeV	SEU
TRIUMF (Canada)	Proton	400 MeV	Basic and applied research
	Neutron		
Boeing Radiation Effects Lab.	Neutron	14 MeV	Research
Texas A&M	Neutron	14 MeV	Research
Eastman Kodak Research Center	Neutron	14 MeV	Research
Dow Chemical	Neutron	14 MeV	Research
US Naval Academy	Neutron	14 MeV	Research
NIST	Neutron	Thermal Cold	Basic nuclear and solid state research; SEU

Annex D – Neutron and Proton Test Facilities (informative) (cont'd)

Listed in Table D.2, are European facilities that have the capability of supporting SEU studies.

Table D.2 — European facilities potentially useful for SEU work

Institution	Beam Type	Energy Range	Type of Work
The Svedberg Lab at Uppsala University, Sweden (TSL)	Proton Neutron	180 MeV	Basic nuclear research; SEU; Radiation therapy
Cyclotron Institute Louvain, Belgium (CYCLONE)	Proton Neutron	80 MeV	Basic and applied research; SEU; Radiation therapy
Paul Scherrer Institute (PSI), Villigen, Switzerland	Proton Neutron	590 MeV and lower	Basic nuclear research; SEU
Proton Therapy Ctr. (CPO), Orsay, France	Proton	150 MeV	Radiation therapy; SEU
Shell Research & Tech. Amsterdam, Netherlands	Neutron	14 MeV	Research
Delft Univ. of Tech. Amsterdam, Netherlands	Neutron	14 MeV	Research
French Central Agency of Arming, France	Neutron	2, 5, & 14 MeV	Research, SEU
French Agency of Atomic Energy, Valduc, France	Neutron	2, 5, 6 & 14 MeV	Research, SEU
Leon Brillouin Institute Saclay, France	Thermal neutron 25 meV flux = 2 x 10^8 n/s cm^2		Research, SEU
Laue-Langevin Institute Grenoble, France	Thermal neutron 25 meV flux = 10^8 n/s cm^2 perfectly monoenergetic		Research, SEU

Table D.3 presents an example of facility usage for the case where a series of mono-energetic sources is used to characterize device sensitivity across the energy regime.

Table D.3 — Monoenergetic Proton Accelerator Facilities for Each Recommended MeV Energy Range (see Tables 5.1 and 5.2)

10-20	50	100	150 MEV
UC Davis	UC Davis	————	————
————	Indiana	Indiana	Indiana
————	————	————	Los Alamos
————	Boston/Harvard	Boston/Harvard	Boston/Harvard
————	Loma Linda	Loma Linda	————
————	TRIUMF	TRIUMF	TRIUMF
	CYCLONE		
————	Svedberg (TSL)	Svedberg (TSL)	Svedberg (TSL)
PSI	PSI	PSI	PSI

Annex E - Calculations of terrestrial neutron flux (normative)

For meaningful comparisons in future SEU work, we need to agree on a method with which we can compute nominal terrestrial neutron flux at an arbitrary location. It is well known that terrestrial neutron fluxes varies as the atmospheric conditions changes. The computing method must be simple to use but at the same time must yield realistic results.

We provide two methodologies that are well documented, simple to use, and which produces neutron fluxes that are close to measure data. For full details, the interested reader can refer to the IBM Journal of Research and Development, vol. 40, No. 1, January 1996, and the NASA-Langley neutron flux model (NASA RP –1257, *Transport Methods and Interactions for Space Radiation*, J. Wilson, et al, 1991, Chapter 13).

First, the cosmic ray neutron flux varies with three main factors: altitude, location (due to variations in the earth's magnetic field) and solar activity (affect the intensity of the cosmic rays reaching the earth). For purposes of the two models, the altitude, a, in feet above sea level, is expressed as the areal density of the air column, A, in units of g/cm^2. The altitude, a, can be converted to the areal density, A using Eq. 1:

$$A = 1033\times\exp[-.03813\times(a/1000) -.00014\times(a/1000)^2 +6.4E\text{-}7\times(a/1000)^3] \qquad (1)$$

For purposes of the models, the most relevant parameter characterizing the geomagnetic interaction with the cosmic rays is the geomagnetic rigidity cutoff, R. Table E.1-B lists the geomagnetic cutoffs for 10 cities around the world. However, in order to provide geomagnetic rigidities for an arbitrary city, Annex E is provided. Once a city is specified in terms of its geographical latitude and longitude, Annex E provides a procedure for calculating the rigidity cutoff, R, for that city. The procedure is based on a 36×24 array of rigidity cutoffs as determined by Smart and Shea (every 5° latitude and 15° longitude) and is good to an accuracy of about 5%.

E.1 IBM method

Once A and R is determined for the city of interest, the IBM method proceeds as follows:

To calculate the nominal neutron flux (in units of neutrons/(cm**2-MeV-s)), there are three steps.

Step 1: Compute the nominal neutron flux, NF0 (neutrons/(cm**2-MeV-s)), of a reference city. For convenience, we use New York City (NYC) as the reference city. The choice of the reference city is arbitrary. In practice, it turns out that the theoretical curve fits a large number of data points that apply to New York City. This (reference) curve is shown in Table E.1-A (or Figure 1A) which gives neutron energy versus differential flux. The neutron energy covers a wide range from 1 MeV up to 10 GeV.

Step 2: Evaluate the altitude effect. In practice, it is easier to do this by converting the altitude, a (feet above sea level), to the areal density, A (g/cm^2) by using Eq. (1). The neutron flux, NF, of the city of interest, is related to the flux, NF1, at another reference altitude (areal density), as

$$NF/NF1 = \exp (- (A-A1)/L) \qquad (2)$$

E.1 IBM method (cont'd)

where :

A is the areal density of the city of interest

A1 is the areal density of NYC (reference city).;

L is the flux attenuation length for neutrons in the atmosphere, also given in units of g/cm^2. For terrestrial neutrons, a good value for L is 148 g/cm^2.

Step 3: Make a final correction according to geomagnetic rigidity. Convert the geographical latitudes and longitudes of the city of interest and NYC into geomagnetic coordinates using Annex E to calculate the geomagnetic rigidities of these two locations.

Table E.1-B (or Figure 1B) shows the relative nucleon flux versus rigidity. The higher curve corresponds to times of minimal solar activity when the cosmic rays, and hence the neutrons, are at their peak, and the lower curve corresponds to the times of high solar activity when the neutron flux is at its minimum. The curve for any year can be interpolated between these two extreme cases. The geomagnetic rigidities and altitudes of a number of cities are compiled in Table E.1-C.

Combining Steps 1 - 3, we arrive at the final result:

Neutron Flux of City of Interest (n/cm²-MeV-s) = (Relative N Flux of City of Interest/ Relative N Flux of NYC) * exp [- (Altitude of City of Interest - Altitude of NYC) / L] * Nominal Flux at NYC

In the first factor on the right side of the above equation, the ratio of the relative fluxes is obtained from Table E.1-B (or Figure 1B). In the second factor, the altitudes (areal densities) are given in g/cm^2, and L = 148 g/cm^2. The nominal flux is obtained from Table E.1-A (or Figure 1A).

E.2 NASA-Langley method

The NASA-LaRC model developed by Wilson, Nealy and co-workers is quite effective for calculating the 1-10 MeV neutron flux at locations around the world. It too needs input parameters to characterize a location, the areal density, the cutoff rigidity and solar activity. It is based on measurements made in aircraft, and so its values for ground level tend to be too high. However, it has been found that an accurate ratio between the cosmic ray neutron flux at 40,000 ft and ground level is 300. Thus one procedure for using the NASA-LaRC model for any city of interest is to calculate the 1-10 MeV flux at 40,000 ft, and divide by 300 (multiply by 3.3E-3) to obtain the ground level neutron flux for neutrons in the 1-10 MeV energy range. The neutron flux at other energies can be obtained by using the nominal neutron flux at sea level contained in Table E.1-A. The last entry in Table E.1-A contains the integrated 1-10 MeV neutron flux (integration of flux over the energy range of 1-10 MeV, first 10 entries in the table). Thus for a city of interest at sea level, the neutron flux would be the values in Table E.1-A multiplied by the ratio of (3.3E-3 ×1-10 MeV flux calculated by the NASA-LaRC model at 40,000 ft)/ (1-10 MeV flux in Table E.1-A).

E.2 NASA-Langley method (cont'd)

One of the advantages of the NASA-Langley model is that it directly allows for the inclusion of the effect of solar activity as represented by the readings of one of the cosmic ray neutron monitors that are located around the world. A convenient one is the monitor at Climax, Colorado (rigidity cutoff of 3 GV) that is operated by the University of Chicago. It has records going back to the 1950s, and its daily readings are accessible on the Internet, (ulysses.uchicago.edu/NeutronMonitor/neutron_mon.html). For the day of interest, the NASA-Langley model requires an input parameter that is the neutron monitor's reading, given as a percentage of the highest value ever recorded by that monitor. The highest value recorded for the Climax monitor is 4418 on March 20, 1987, indicating minimal solar activity. Thus for March 20, 1987 the solar activity parameter would be 100, and for January 1, 1991, a time of high solar activity, a low value of 3662 was recorded [input parameter of 83, (3662/4418)×100].

E.3 Shielding considerations

The above equations give the nominal neutron flux to which the device or circuit is exposed without shielding. However in most applications at sea level the materials of the building attenuate the actual flux that impinges on the electronics. Due to this shielding, most of the low-energy components (in the MeV range or below) of the neutron flux is absorbed.

The high-energy components (tens of MeV and above) are attenuated, but penetrate the building materials. The absorption of neutrons in ordinary concrete can be roughly estimated to be an empirical attenuation factor of 1.4 for every foot of concrete, or attenuation = exp (-0.35x) where x is the concrete thickness in feet.

In situations, say in an airplane, where the shielding of the surrounding materials is much less effective than concrete, low-energy neutrons can hit the system and can induce soft fails.

Table E.1-A — Nominal (Theoretical) Neutron Flux at Sea Level

Neutron Energy (MeV)	Differential Flux*		Neutron Energy (MeV)	Differential Flux*		Neutron Energy (MeV)	Differential Flux*
1	2.30E-03		60	1.69E-05		2,000	3.03E-08
2	9.30E-04		70	1.41E-05		3,000	1.09E-08
3	5.47E-04		80	1.20E-05		4,000	5.13E-09
4	3.76E-04		90	1.03E-05		5,000	2.83E-09
5	2.81E-04		100	8.97E-06		6,000	1.73E-09
6	2.21E-04		200	3.30E-06		7,000	1.14E-09
7	1.81E-04		300	1.69E-06		8,000	7.94E-10
8	1.52E-04		400	1.01E-06		9,000	5.76E-10
9	1.30E-04		500	6.59E-07		10,000	4.32E-10
10	1.14E-04		600	4.59E-07			
20	5.52E-05		700	3.34E-07		1-10	3.8E-3
30	3.63E-05		800	2.52E-07			
40	2.68E-05		900	1.95E-07			
50	2.09E-05		1,000	1.55E-07			

* The units for Differential Flux are "#/(cm^2-MeV-s)"

Annex E - Calculations of terrestrial neutron flux (normative) (cont'd)

Table E.1-B — Relative Nucleon Flux vs Geomagnetic Rigidity

	Relative Nucleon Flux				Relative Nucleon Flux	
Geomagnetic Rigidity (GV)	Quiet Sun Peak	Active Sun Minimum		Geomagnetic Rigidity (GV)	Quiet Sun Peak	Active Sun Minimum
0.0	1.000	0.720		8.0	0.750	0.540
1.0	0.998	0.715		9.0	0.705	0.510
2.0	0.985	0.705		10.0	0.665	0.480
3.0	0.960	0.690		11.0	0.625	0.450
4.0	0.930	0.670		12.0	0.595	0.430
5.0	0.890	0.640		13.0	0.570	0.410
6.0	0.845	0.610		14.0	0.555	0.400
7.0	0.800	0.580				

Table E.1-C — Geomagnetic Rigidity and Altitude of Several Cities

City	**Geomagnetic Rigidity (GV)**	**Altitude (ft)**	**Areal Density (G/cm^2)**
U.S. East Coast			
Boston, MA	1.7	0	1033
New York City, NY	1.9	0	1033
Washington, DC	2.2	0	1033
Miami, FL	5.3	0	1033
U.S. West Coast			
Anchorage, AK	0.98	0	1033
San Diego, CA	6.0	0	1033
Seattle, WA	1.3	0	1033
Higher Altitude U.S. Cities			
Albuquerque, NM	4.4	4945	863
Chicago, IL	2.1	595	1011
Denver, CO	2.7	5,280	851
Leadville, CO	2.7	10,200	710
International Cities			
London, UK	3.1	245	1024
Sidney, Australia	4.9	0	1033
Tokyo, Japan	12.0	0	1033

Annex F - Procedure for Calculating the geomagnetic rigidity cutoff for an arbitrary city (normative)

Its geographical latitude and longitude characterize an arbitrary city, C. The purpose of this procedure is to calculate the geomagnetic rigidity cutoff, R, for the city, based on its latitude and longitude. To do this, we will use the tabulation of geomagnetic rigidity cutoffs compiled by Smart and Shea (see Ref.), and which are incorporated into the CREME computer code. Longitude can be expressed either in terms of Longitude East or Longitude West. The rigidity cutoff tabulation is based on Longitude East, so all longitudes have to be expressed in this convention. Thus, while New York City may be identified as being at 74° longitude west, for these purposes the relevant latitude is 286° longitude east. The tabulation consists of a 36×24 array of rigidity cutoffs (every 5° latitude and 15° longitude), and is found in Table F.1 and F.2 (they are divided into two tables because of the large amount of data, 864 rigidity values).

The rigidity cutoff will be calculated based on an interpolation using the rigidity values for the bounding longitude and latitude combinations. Thus if C has a latitude value of Y and a longitude east value of Z, the bounding latitudes Lat0 and Lat1 and the bounding east longitudes Lon0 and Lon1 have to be determined. Once they are determined, the rigidity values at the four locations (Lon0- Lat0, Lon0-Lat1, Lon1-Lat0 and Lon1-Lat1) are obtained from the tables, and these are R00, R01, R10 and R11. The rigidity, R, for city C is then obtained by interpolation with these four rigidity values. To carry out the interpolation, the following two fractions are defined: p = (Z-Lon0)/(Lon1-Lon0) and q = (Y-Lat0)/(Lat1-Lat0). Then the rigidity, R, for C is given by:

$$R = (1-p)\times(1-q)\times R00 + p(1-q)\times R10 + q(1-p)\times R01 + pq\times R11$$

In practice this interpolation scheme is accurate to within about 5%.

References:

M. A. Shea and D. F. Smart, *“The Influence of the Changing Geomagnetic Field on Cosmic Ray Measurements,”* J. Geomag. Geoelect., 62, 1107 (1990)

J. H. Adams, Jr., "Cosmic Ray Effects on Microelectronics (CREME)," NRL Memorandum 5901, 1986

Annex F - Procedure for Calculating the geomagnetic rigidity cutoff for an arbitrary city (normative) (cont'd)

Table F.1 — Vertical Rigidity Cutoffs in GV at 20 km Altitude, 0-165° Longitude East

Latitude	Longitude East											
	0	**15**	**30**	**45**	**60**	**75**	**90**	**105**	**120**	**135**	**150**	**165**
90	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04
85	0.03	0.04	0.05	0.06	0.06	0.07	0.07	0.07	0.07	0.07	0.06	0.05
80	0.02	0.04	0.06	0.09	0.09	0.10	0.10	0.11	0.11	0.11	0.08	0.06
75	0.10	0.14	0.18	0.20	0.23	0.25	0.25	0.26	0.27	0.28	0.26	0.24
70	0.26	0.34	0.41	0.47	0.49	0.51	0.52	0.55	0.59	0.60	0.62	0.56
65	0.58	0.72	0.80	0.89	0.93	0.97	1.01	1.03	1.12	1.19	1.20	1.13
60	1.14	1.34	1.46	1.57	1.61	1.67	1.73	1.82	1.95	2.05	2.05	1.99
55	1.94	2.28	2.47	2.61	2.68	2.78	2.85	2.92	3.12	3.31	3.35	3.15
50	3.21	3.54	3.81	3.97	4.14	4.27	4.36	4.37	4.68	4.93	4.92	4.67
45	4.77	5.12	5.36	5.51	5.73	5.90	6.11	6.29	6.57	6.86	6.86	6.33
40	6.75	7.27	7.48	7.70	8.19	8.73	9.14	9.29	9.49	9.89	9.74	8.95
35	9.54	9.89	10.10	10.53	11.15	11.44	11.52	11.71	11.93	12.04	11.55	10.60
30	11.30	11.71	12.13	12.67	13.34	14.07	14.37	14.40	14.26	13.95	13.44	12.72
25	13.10	13.64	14.10	14.53	15.06	15.58	15.85	15.79	15.49	15.03	14.44	13.76
20	14.11	14.62	15.09	15.57	16.12	16.63	16.87	16.75	16.37	15.83	15.20	14.55
15	14.61	15.14	15.65	16.17	16.74	17.25	17.47	17.34	16.93	16.37	15.76	15.17
10	14.73	15.26	15.80	16.34	16.94	17.44	17.67	17.56	17.18	16.65	16.10	15.61
5	14.50	14.99	15.52	16.10	16.71	17.22	17.47	17.42	17.11	16.66	16.21	15.83
0	13.94	14.37	14.87	15.46	16.10	16.62	16.90	16.94	16.73	16.38	16.05	15.81
-5	13.13	13.45	13.91	14.50	15.14	15.65	15.97	16.10	16.00	15.77	15.58	15.50
-10	12.11	12.31	12.71	13.29	13.89	14.35	14.68	14.90	14.91	14.80	14.74	14.84
-15	10.75	10.91	11.23	11.69	12.18	12.70	13.00	13.25	13.25	13.32	13.48	13.78
-20	9.21	9.06	9.29	9.70	10.21	10.25	10.41	10.65	10.84	10.62	10.74	11.93
-25	7.55	7.50	7.72	7.88	7.86	7.37	7.08	7.24	7.43	7.71	8.47	9.55
-30	6.36	6.02	5.86	5.79	5.42	5.23	5.10	5.16	5.19	5.39	5.89	6.58
-35	5.24	4.59	4.45	4.31	4.07	3.72	3.35	3.32	3.37	3.65	4.10	4.90
-40	4.29	3.74	3.40	3.21	2.83	2.43	2.08	2.00	2.01	2.21	2.65	3.24
-45	3.46	2.96	2.53	2.30	1.93	1.53	1.28	1.12	1.11	1.25	1.51	2.04
-50	2.87	2.37	1.95	1.60	1.27	0.94	0.66	0.54	0.53	0.60	0.84	1.15
-55	2.23	1.79	1.42	1.12	0.87	0.53	0.34	0.23	0.21	0.26	0.38	0.59
-60	1.78	1.32	1.03	0.75	0.49	0.30	0.15	0.08	0.06	0.08	0.14	0.27
-65	1.30	0.98	0.72	0.50	0.30	0.15	0.06	0.00	0.00	0.00	0.03	0.11
-70	0.89	0.64	0.47	0.31	0.18	0.08	0.00	0.00	0.00	0.00	0.00	0.03
-75	0.59	0.43	0.30	0.19	0.10	0.04	0.00	0.00	0.00	0.00	0.00	0.00
-80	0.37	0.28	0.19	0.13	0.07	0.03	0.00	0.00	0.00	0.00	0.00	0.00
-85	0.29	0.24	0.20	0.17	0.14	0.12	0.10	0.10	0.10	0.10	0.10	0.10
-90	0.21	0.21	0.21	0.21	0.21	0.21	0.21	0.21	0.21	0.21	0.21	0.21

Annex F - Procedure for Calculating the geomagnetic rigidity cutoff for an arbitrary city (normative) (cont'd)

Table F.2 — Vertical Rigidity Cutoffs in GV at 20 km Altitude, 180-360° Longitude East

Latitude	**Longitude East**												
	180	**195**	**210**	**225**	**240**	**255**	**270**	**285**	**300**	**315**	**330**	**345**	**360**
90	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04
85	0.04	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.03
80	0.04	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.02
75	0.20	0.14	0.09	0.03	0.00	0.00	0.00	0.00	0.00	0.00	0.02	0.07	0.10
70	0.47	0.36	0.23	0.13	0.06	0.00	0.00	0.00	0.00	0.05	0.11	0.18	0.26
65	0.95	0.74	0.53	0.32	0.17	0.09	0.05	0.04	0.08	0.16	0.28	0.42	0.58
60	1.75	1.40	1.00	0.65	0.40	0.22	0.16	0.14	0.21	0.38	0.59	0.86	1.14
55	2.88	2.22	1.75	1.23	0.78	0.50	0.36	0.36	0.46	0.75	1.13	1.59	1.94
50	4.27	3.38	2.81	2.03	1.41	0.95	0.73	0.69	0.89	1.34	1.98	2.65	3.21
45	5.59	4.85	4.08	3.16	2.37	1.74	1.32	1.22	1.49	2.21	3.16	4.20	4.77
40	7.86	6.46	5.41	4.55	3.61	2.76	2.07	1.93	2.42	3.41	4.82	5.92	6.75
35	9.49	8.97	7.65	6.12	5.21	4.25	3.19	2.89	3.58	4.98	6.80	8.70	9.54
30	11.65	10.48	9.63	8.78	7.00	5.60	4.44	4.07	4.87	6.98	9.67	10.60	11.30
25	13.07	12.43	11.81	10.98	9.74	7.89	6.08	5.44	6.56	9.65	11.47	12.46	13.10
20	13.93	13.40	12.91	12.33	11.47	9.69	7.82	6.84	8.65	11.45	12.76	13.54	14.11
15	14.63	14.16	13.76	13.30	12.62	11.27	9.49	8.46	10.71	12.52	13.43	14.07	14.61
10	15.16	14.75	14.39	14.00	13.44	12.55	11.50	11.07	12.16	13.09	13.76	14.25	14.73
5	15.49	15.15	14.82	14.47	14.03	13.41	12.67	12.40	12.78	13.36	13.80	14.11	14.50
0	15.59	15.32	15.03	14.71	14.33	13.06	13.32	12.95	13.05	13.38	13.58	13.69	13.94
-5	15.42	15.25	15.02	14.74	14.41	14.01	13.53	13.14	13.08	13.19	13.15	13.04	13.13
-10	14.94	14.90	14.76	14.55	14.29	13.94	13.51	13.10	12.92	12.82	12.55	12.20	12.11
-15	14.09	14.24	14.24	14.15	13.97	13.69	13.30	12.89	12.59	12.31	11.76	11.15	10.75
-20	12.78	13.19	13.44	13.51	13.46	13.28	12.94	12.53	12.14	11.65	10.73	9.78	9.21
-25	10.22	11.22	12.01	12.63	12.76	12.72	12.46	12.04	11.53	10.74	9.63	8.36	7.55
-30	7.99	9.45	9.43	10.64	11.85	12.00	11.88	11.43	10.75	9.83	8.39	7.09	6.36
-35	5.65	6.54	7.88	9.11	9.58	11.12	11.16	10.67	9.90	8.72	7.16	6.18	5.24
-40	4.11	4.76	5.56	6.65	8.20	9.75	10.18	9.77	8.98	7.61	6.42	5.31	4.29
-45	2.72	3.33	4.24	4.93	5.91	7.83	9.00	8.76	7.84	6.91	5.63	4.32	3.46
-50	1.63	2.24	2.94	3.76	4.48	5.57	7.02	7.57	6.98	5.68	4.51	3.50	2.87
-55	0.90	1.38	1.88	2.64	3.38	4.20	4.96	5.19	5.02	4.45	3.67	2.93	2.23
-60	0.48	0.79	1.18	1.62	2.23	3.00	3.77	3.95	3.97	3.52	2.88	2.27	1.78
-65	0.23	0.43	0.71	1.06	1.51	1.98	2.53	2.71	2.72	2.50	2.10	1.61	1.30
-70	0.10	0.22	0.41	0.64	0.96	1.24	1.58	1.75	1.80	1.67	1.39	1.14	0.89
-75	0.05	0.12	0.23	0.36	0.54	0.72	0.91	1.02	1.03	1.05	0.88	0.76	0.59
-80	0.03	0.08	0.13	0.21	0.30	0.40	0.48	0.55	0.56	0.54	0.49	0.42	0.37
-85	0.12	0.14	0.17	0.21	0.25	0.30	0.34	0.38	0.38	0.37	0.35	0.31	0.29
-90	0.21	0.21	0.21	0.21	0.21	0.21	0.21	0.21	0.21	0.21	0.21	0.21	0.21

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